B
S02

2-E-24

VIKING LABORATORIES INC

TECHNICAL MANUAL

MODEL 784

TIME INTERVAL COUNTER

technical manual

MP MASTER
MA29723

ELDORADO
ELDORADO ELECTRODATA CORPORATION
935 DETROIT AVENUE - CONCORD, CALIF. 94518 U.S.A. - TEL. (415) 686-4200 - TWX 910-481-9476

TECHNICAL MANUAL

MODEL 784

TIME INTERVAL COUNTER

VIKING LABORATORIES INC.

ELDORADO INSTRUMENTS CO
2495 Estand Way
Pleasant Hill, CA 94523
(415) 682-2100

warranty

Eldorado instruments are warranted during a period of one year from date of shipment to original purchaser to be free from defects in material and workmanship. The liability of Eldorado under this warranty is limited to replacing or repairing any instrument or component thereof which is returned by Buyer and has not been subjected to misuse, neglect, improper installation, repair, alteration, or accident. Eldorado shall have the right of final determination as to the existence and cause of a defect. In no event shall Eldorado be liable for collateral or consequential damages. ~~In order to expedite the rapid turnaround of your unit, please obtain a Returned Material Authorization (RMA) number by contacting the Customer Service Department. In all correspondence or telephone calls, a model number and serial number is required. Address all correspondence to Customer Service Department, Eldorado Electrodata Corporation, 601 Chalomar Road, Concord, California 94520, Phone (415) 686-4200, TWX 910 481 9476.~~

The instrument should be shipped prepaid with the return form attached to the packing container. When the instrument is repaired it will be returned to you best way prepaid.

This warranty is in lieu of any other warranty, express, implied, or statutory, and no agreement extending or modifying it will be binding upon Eldorado unless in writing and signed by a duly authorized officer.

RECEIVING INSPECTION

Every Eldorado instrument is carefully inspected and is in perfect working order at the time of shipment. Each instrument should be checked as soon as received. If the instrument is damaged in any way or fails to operate, a claim should immediately be filed with the transportation company. In any case where damage occurs in transit with the instrument in packing case, Eldorado's obligations under warranty are dependent on the customer's immediately notifying the carrier so that inspection can be made and a claim filed.

REPAIR SERVICE

Experienced service personnel and special test equipment are available at the factory to perform any necessary repairs. Every effort will be made to expedite the repair of instruments returned for servicing. Repair work will be performed only upon receipt of a written purchase order or authorization. Utilize the same procedure for returning an instrument for service as for warranty return. After receipt of the unit the Customer Service Department will issue a quotation of repair costs for your approval.

INITIAL TESTING OF UNHEATED CRYSTAL OSCILLATORS
(Non-Ovenized)

Extensive testing of the aging rates of the unheated type crystal oscillators has recently been completed. Based on this research, verification of the published aging rate can be accurately determined within a reduced time interval. The following procedure will validate the initial aging specifications.

1. Attach a thermometer or temperature sensing device to the crystal case.

2. Apply instrument power for a twenty four hour period.

3. Measure the crystal's external temperature to within 1° C.

4. Measure the crystal oscillator's frequency to within 1 part in 10^7 (0.1 Hz).

5. After one week's continuous operation again measure the crystal temperature and output frequency.

6. The two frequencies will be within 2 parts in 10^6 (2 Hz), taking into consideration a temperature coefficient of $\pm 0.5 \times 10^{-6}$/° C.

7. The above test confirms the published oscillator specifications.

The information necessary to complete this page appears on the serialized name plate located on the rear panel of the instrument.

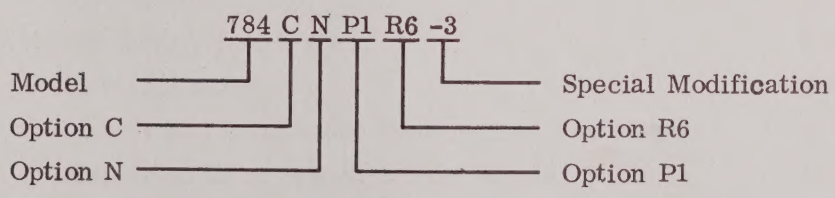
This manual is packaged with Model 784 Serial Number _____ and is applicable to instruments with serial number 157 and above.

The following options are incorporated into this instrument:

Option C ☐
Option C1 ☐
Option N ☐
Option P1 ☐
Option R6 ☐
Option R8 ☐

Special Modification Number _____.

Model Number and Option Legend



Digitized by the Internet Archive
in 2025

https://archive.org/details/manualsplus_07424

TABLE OF CONTENTS

		PAGE
SECTION 1	GENERAL INFORMATION	
1.1	Introduction	1-1
1.2	Specifications	1-1
SECTION 2	INSTALLATION AND OPERATION	
2.1	Introduction	2-1
2.2	Unpacking and Inspection	2-1
2.3	Power Requirements	2-1
2.4	Incoming Confidence Check	2-2
2.5	Installation	2-3
2.6	Front Panel Description	2-10
2.7	Rear Panel Description	2-12
2.8	Operation	2-15
SECTION 3	THEORY OF OPERATION	
3.1	Introduction	3-1
3.2	Block Diagram Analysis	3-1
3.3	Circuit Analysis	3-3
SECTION 4	MAINTENANCE AND CALIBRATION	
4.1	Introduction	4-1
4.2	Periodic Maintenance	4-2
4.3	Calibration	4-2
4.4	Internal Adjustments	4-4
4.5	Fault Isolation	4-7
4.6	Repair and Component Replacement Techniques	4-11
4.7	Replacement of Selected Components	4-12
4.8	Integrated Circuit Equivalents	4-13
SECTION 5	PARTS LIST	
5.1	Introduction	5-1
5.2	Ordering Information	5-1
5.3	Code of Manufactures	5-1
SECTION 6	SCHEMATICS AND RELATED DRAWINGS	

LIST OF ILLUSTRATIONS

FIGURE	TITLE	PAGE
2-1	Option R6 Rack Mount Assembly	2-7
2-2	Option R8 Rack Mount Assembly	2-9
2-3	Front Panel	2-14
2-4	Rear Panel	2-14
3-1	Simplified Block Diagram	3-15
4-1	1 MHz Time Base Standardization Test Configuration	4-3
4-2	Trigger Symmetry Adjustments Configuration	4-6
4-3	CμL958 Equivalent	4-14
4-4	CμL959 Equivalent	4-15
4-5	CμL960 Equivalent	4-16
4-6	MC824P Equivalent	4-17
4-7	MC826P Equivalent	4-18
4-8	MC836P Equivalent	4-19
4-9	MC840P Equivalent	4-20
4-10	MC1004P Equivalent	4-21
4-11	MC1010P Equivalent	4-22
4-12	MC1013P Equivalent	4-23
4-13	MC1017P Equivalent	4-24
4-14	MC1023P Equivalent	4-25
4-15	MC1027P Equivalent	4-26
4-16	MC1039 Equivalent	4-27
4-17	MC1812P Equivalent	4-28
4-18	MC9802P Equivalent	4-29
4-19	N8280A Equivalent	4-30
4-20	SC7355P Equivalent	4-31
6-1	Schematic, Input Circuit (D-11-06226F)	6-1
6-2	Schematic, Steering Logic (D-11-06227H)	6-2
6-3	Schematic, Count Chain and Reset Circuitry (D-11-06228G)	6-3
6-4	Schematic, 100 MHz VCO (C-11-06229F)	6-4
6-5	Schematic, "P" Option (C-11-06226B)	6-5

List of Illustrations (continued)

FIGURE	TITLE	PAGE
6-6	Schematic, Power Supply (C-11-06226B)	6-6
6-7	Logic Display P.C. Board, Component Location Diagram	6-7
6-8	VOC P.C. Board, Component Location Diagram	6-8
6-9	Heatsink Subassembly, Component Location Diagram	6-9
6-10	Front and Rear Panel, Component Location Diagram	6-10
6-11	"P" Option P.C. Board, Component Location Diagram	6-11

LIST OF TABLES

TABLE	TITLE	PAGE
1-1	Specifications	1-2
2-1	230 Volt Operation	2-2
2-2	Confidence Check	2-3
2-3	Data Output Pin Assignments	2-5
2-4	Option R6 Rack Mount Assembly	2-6
2-5	Option R8 Rack Mount Assembly	2-8
2-6	Front Panel Assembly	2-10
2-7	Rear Panel Assembly	2-12
2-8	Time Interval Measurement	2-15
2-9	Period Measurement	2-16
2-10	Pulse Width Measurement	2-17
2-11	Cable Length Measurement	2-19
4-1	Recommended Test Equipment	4-1
4-2	Time Base Standardization	4-3
4-3	VCO Phaselock Adjustment	4-5
4-4	Trigger Symmetry Adjustment	4-6
4-5	Model 784 Sectionalization	4-8
5-1	Code of Manufacturers	5-2

SECTION 1

GENERAL INFORMATION

SECTION 1

GENERAL INFORMATION

1.1 INTRODUCTION

The Eldorado Model 784 Time Interval Counter is a precision digital instrument capable of measuring intervals of time with 1 nanosecond effective resolution. The instrument can measure the time interval between two separate signals or the period of a single input in either a normal (X1) or expanded (X1000) operating mode. In the X1 mode, measurements from 000000.01 microseconds to 999999.99 microseconds are realized with 10 nanosecond resolution while in the X1000 mode, measurements from 000.010 microseconds to 999.999 microseconds are possible with 1 nanosecond effective resolution. The instrument can be readily adapted to pulse width and rise time measurements by paralleling the start input with the stop input by means of a BNC tee and additional section of cable.

Individual input channels with separate slope, trigger level and attenuation controls provide complete input signal conditioning for all measurement functions. Input signals from 100 mV to 100 volts can be measured by appropriate selection of the level control and attenuation factor. Measurements are displayed directly in microseconds on a row of eight numerical indicator tubes with automatically positioned decimal point. A stored type display is featured with the display time variable from 0.1 seconds to 10 seconds or infinite as determined by the front panel display control. External trigger monitors for the start and stop channels are provided on the rear panel to facilitate locating the desired trigger points on the input waveform.

While ideally suited to a bench type environment, the availability of optional rear inputs, digital output and rack mounting combined with the standard remote reset feature further increases the Model 784's versatility to include systems oriented applications.

1.2 SPECIFICATIONS

Specifications for the Model 784 are outlined in Table 1-1.

TABLE 1-1 (Continued)

	Frequency:	1 MHz
	Aging:	± 1 part in 10^6 per month after 30 days operation.
	Temperature:	± 0.002% from 0°C to +50°C.
GENERAL		
	Display:	8 digits, in the X1 mode, 6 digits, in the X1000 mode, of numerical indicators and gate lamp. Display reads directly in microseconds with automatically positioned decimal point.
	Reset:	Automatic; 0.1 seconds to 10 seconds or infinite by front panel display control. Manual; Front panel momentary pushbutton switch. Remote; Rear panel subminature connector by positive pulse going pulse +3 to +10 volts amplitude, 20 kHz maximum repetition rate.
	Temperature:	Operating; 0°C to +50°C. Storage; -55°C to +80°C.
	Power Requirements:	115 or 230Vac (± 10%), 48-62 Hz, 50 watts.
	Dimensions:	3.5" x 8.4" x 11.0" (HxWxD).
	Weight:	8 lbs. net. 13 lbs. shipping.

TABLE 1-1 (Continued)

OPTIONS	
Option C:	Internal temperature control crystal oscillator (115 volt operation). Short Term Stability: ±7 parts in 10^9 (average) over 10 s period. Long Term Stability: ±3 parts in 10^8 per week after 45 days operation. Temperature: ±5 parts in 10^9 per ° C from 0° C to +50° C.
Option C1:	Internal temperature control crystal oscillator (230 volt operation). Short Term Stability: ±7 parts in 10^9 (average) over 10 s period. Long Term Stability: ± 3 parts in 10^8 per week after 45 days operation. Temperature: ±5 parts in 10^9 per ° C from 0° C to +50° C.
Option N:	Rear panel mounted start and stop input connector.
Option P1:	Micrologic 1-2-4-8 BCD output, positive zone, positive true logic.
Option R6:	Rack mounting hardware for mounting single instrument in standard 19 inch rack width.
Option R8:	Rack mounting hardware for mounting two instruments, side-by-side, in standard 19 inch rack width.

SECTION 2

INSTALLATION AND OPERATION

SECTION 2

INSTALLATION AND OPERATION

2.1 INTRODUCTION

This section describes the unpacking, inspection, installation, and operational procedures for the Model 784 Time Interval Counter.

2.2 UNPACKING AND INSPECTION

Upon receipt of the instrument from the shipper, inspect the shipping container for external damage incurred during transit. Any indication of such damage must be noted by both the shipper and customer, and should be reported to the insurance investigator immediately.

Remove the instrument from the packing case and visually inspect it for obvious physical damage (scratches, dents, broken fittings, etc). In the event of damage, notify the factory or your nearest Eldorado representative - Do NOT attempt to use the instrument as electrical damage may result.

Every instrument is shipped with an instruction manual. Verify any specified options or modifications against your purchase order. Changes or special modifications are described by a yellow addendum located at the front of the manual.

2.3 POWER REQUIREMENTS

The instrument is equipped with an attached standard 3 prong (NEMA) line cord that automatically grounds the instrument chassis when terminated to a grounded power receptacle. An adapter providing an instrument ground must be used whenever termination to a biterminal outlet is necessitated.

The Model 784 is capable of operating from either a 115 or 230 volt ac, 48-62 Hz source. The instrument is normally shipped for 115 volt operation.

If operation from a 230 volt ac source is desired, follow the steps outlined in Table 2-1.

CAUTION

The optional high stability oscillators are designed to function only from a specified source voltage. Under no circumstances attempt to change the 115/230 volt line switch setting when either Option C or Option C1 is installed within the instrument.

TABLE 2-1

230 VOLT OPERATION

STEP	ACTION
1	Slide the POWER switch to the OFF position and remove the line cord from the source.
2	Slide the rear panel 115/230 volt line switch to the position revealing the numerals 230.
3	To adequately protect the instrument, replace the existing 1 ampere SLO-BLO fuse with a 1/2 ampere SLO-BLO fuse.
4	Conspicuously label the instrument for 230 volt operation.

2.4 INCOMING CONFIDENCE CHECK

Prior to packaging the instrument for shipment, extensive operational, alignment and calibration checks were performed. To satisfy electrical integrity of the instrument at the receiving bench, a simple confidence check can be performed. This check requires no additional equipment and is intended only to verify basic operation. Prior to performing the confidence check, it is recommended that the operator become familiar with the basic operating controls described in paragraphs 2.6 and 2.7. Table 2-2 outlines the confidence check.

TABLE 2-2

CONFIDENCE CHECK

STEP	ACTION
1	Referring to paragraph 2.3, connect the line cord to an appropriate power source.
2	Verify that the rear panel INT/EXT switch is in the INT. position.
3	Slide the power ON switch to the ON position and note that the display illuminates and the fan is energized.
4	Set the DISPLAY TIME control to mid range, slide the START and STOP SLOPE switches to "+" and rotate the MODE - MODE X1000 switch to the TIME INT. (X1) position.
5	Rotate the START and STOP LEVEL controls fully clockwise and depress the RESET pushbutton switch. The display will indicate all zeros.
6	Slowly rotate the START LEVEL control in a counter-clockwise direction until the GATE lamp illuminates. This will occur at approximately mid-range
7	Rotate the STOP LEVEL control counter-clockwise until the GATE lamp extinguishes. The display will indicate a random number which can be cleared by depressing the RESET pushbutton switch.

2.5 INSTALLATION

The Model 784 is operable upon receipt requiring only the connection of suitable inputs and the termination of the line cord to a proper ac power source. A self-locking elevating bail is attached to the front "feet" to elevate the front panel for more convenient viewing.

2.5.1 Installation Considerations

Cooling is provided by a rear panel mounted fan. The air intake duct must remain unobstructed and sufficient rear panel clearance must be maintained to assure adequate air circulation. This consideration is also valid for rack mount installations.

2.5.2 Data Output

If the binary coded decimal (BCD) output (Option P1) is incorporated into the instrument, refer to the following table for individual pin assignments and binary translations for the rear panel digital output connector. All data outputs are positive zone, positive true with logic "0" equal to 0 volts (±0.3V) and logic "1" equal to +5 volts (±0.7V). The positive print command, at the conclusion of the count cycle, is a positive going pulse from 0 volts to +5 volts (nominal) with a rise time greater than 1 volt per 1 μs and greater than 20 μs in duration from a 100Ω series resistance.

Positive and negative reset inhibits are also provided. The positive reset inhibit (+) accepts a positive going input step between +2.5 and +15 volts into a 2kΩ source to inhibit reset. Release will occur at return to 0 volts or return to an open circuit. Negative reset inhibit (-) accepts a negative going step to 0 volts or a negative voltage to inhibit reset. Release occurs at return to greater than +1 volt or to an open circuit. The sink current is approximately 3 mA at 0V; a diode clamps negative levels to ground through a 100Ω resistance. The printer output format is LDXXXXXXXX with L representing the legend, D the decimal location from the right and X and numerical data.

NOTE

Although the two least significant digits of the display are blanked in the expanded (X1000) operating modes, the printout will include all eight numerical data outputs.

TABLE 2-3

DATA OUTPUT PIN ASSIGNMENTS

PIN NO.	FUNCTION
1	10^0 1 bit
2	10^0 2 bit
3	10^1 1 bit
4	10^1 2 bit
5	10^2 1 bit
6	10^2 2 bit
7	10^3 1 bit
8	10^3 2 bit
9	10^4 1 bit
10	10^4 2 bit
11	10^5 1 bit
12	10^5 2 bit
13	10^6 1 bit
14	10^6 2 bit
15	10^7 1 bit
16	10^7 2 bit
17	Decimal 1 bit
18	Decimal 2 bit
19	Legend 1 bit
20	Legend 2 bit
21	NC
22	+ Inhibit
23	+ Print Command
24	Neg. Ref. (0V)
25	Pos. Ref. (+5V)

PIN NO.	FUNCTION
26	10^0 4 bit
27	10^0 8 bit
28	10^1 4 bit
29	10^1 8 bit
30	10^2 4 bit
31	10^2 8 bit
32	10^3 4 bit
33	10^3 8 bit
34	10^4 4 bit
35	10^4 8 bit
36	10^5 4 bit
37	10^5 8 bit
38	10^6 4 bit
39	10^6 8 bit
40	10^7 4 bit
41	10^7 8 bit
42	Decimal 4 bit
43	Decimal 8 bit
44	Legend 4 bit
45	Legend 8 bit
46	NC
47	- Inhibit
48	NC
49	NC
50	Ground

BINARY TRANSLATIONS

LEGEND
1 = microseconds

DECIMAL LOCATION		
1 = 1	3 = 3	5 = 5
2 = 2	4 = 4	

2.5.3 Rack Mount Installation

Two rack mount options are available for the Model 784. Option R6 provides the necessary hardware for mounting a single instrument in a standard 19 inch rack while Option R8 enables two similar instruments to be installed, side-by-side, in a standard 19 inch rack width. Assembly of the Option R6 rack mount kit is outlined in Table 2-4 and illustrated in Figure 2-1. All hardware, with the exception of the mounting screws securing the completed assembly to the rack, are included within the kit.

TABLE 2-4

OPTION R6 RACK MOUNT ASSEMBLY

STEP	ACTION
1	Remove the four "feet" and bail from the bottom cover panel.
2	Secure a rack handle to both the rack ear (4805) and extender panel with the supplied #10-32 x 3/8" screws.
3	Remove the two screws securing each side panel to the instrument chassis. These screws may be discarded.
4	Position spacer plates (5347) over the vacant holes and assemble the rack ear to one side and the panel angle to the other side using the supplied #8-32 x 1/2" screws.
5	Secure the extender panel to the panel angle (5108) using the #6-32 x 3/8" screws, split washers and hex nuts.
6	The instrument is now ready for insertion into the rack cavity.

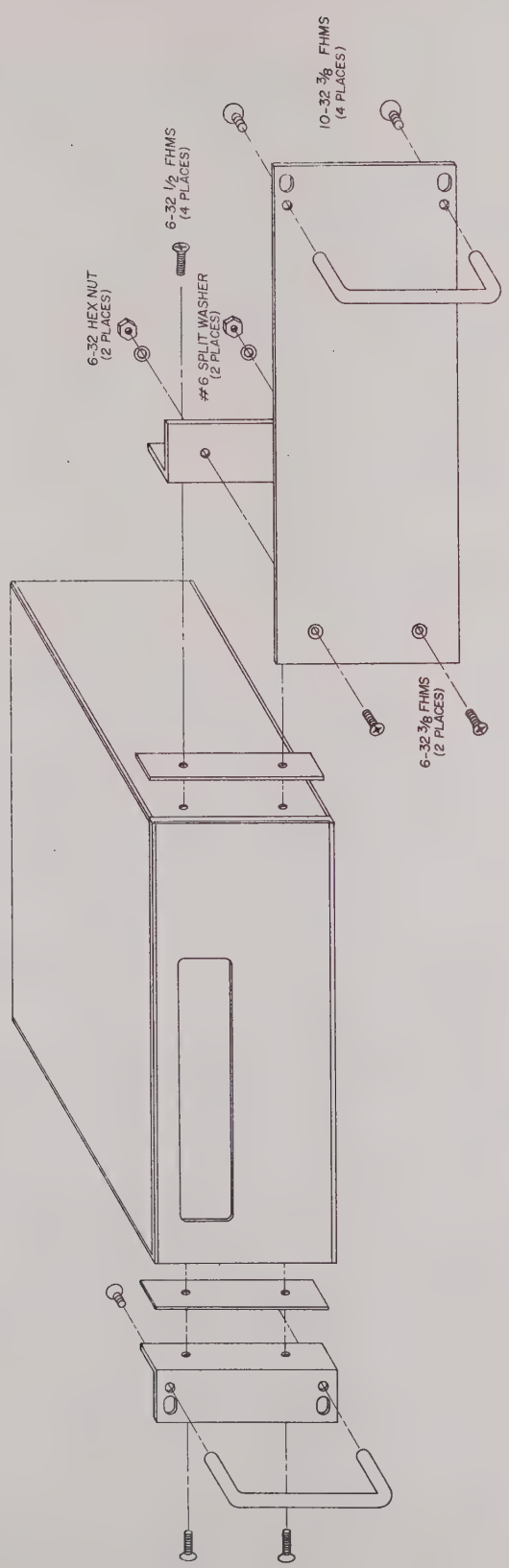


FIGURE 2-1
OPTION R6
RACK MOUNT ASSEMBLY

Assembly of the Option R8 rack mount kit is outlined in Table 2-5 and illustrated in Figure 2-2.

TABLE 2-5
OPTION R8 RACK MOUNT ASSEMBLY

STEP	ACTION
1	Remove the four "feet" and elevating bail from each bottom cover panel.
2	Remove each set of screws securing the side dress panels to the instruments. These screws may be discarded.
3	Secure a rack handle to each rack ear (4805) with the supplied #10-32 x 3/8" screws.
4	Remove the right side dress panel from the instrument to be installed on the left side of the rack. It will be necessary to first remove the carrying handle before the side panel can be removed. This is readily accomplished by prying up the chrome dress covers with a common screwdriver and then removing the two screws securing the handle to the side panel.
5	Remove the left side dress panel from the instrument to be positioned on the right side of the rack .
6	Secure the two instruments together by inserting the panel-filler assembly between the two instruments. NOTE The panel-filler assembly normally does not require securing to the side sub-chassis. If additional security is required, tap sub-chassis with 8-32 size tap and secure in place with #8-32 x 1/4" supplied screws.
7	Position spacer plate (5347) over vacant holes and assemble rack ears to side panels using the supplied #6-32 x1/2" screws.
8	The instruments are now ready for insertion into the rack cavity.

FIGURE 2-2
OPTION R8
RACK MOUNT ASSEMBLY

2.6 FRONT PANEL DESCRIPTION

Table 2-6 and Figure 2-3 describe the front panel controls and functions. The indexed numbers appearing in the left hand column of the table are referenced to individual call-outs appearing on the front panel illustration on page 2-14.

TABLE 2-6
FRONT PANEL DESCRIPTION

INDEX	NOMENCLATURE	FUNCTION
(1)	GATE Lamp	An indicator which illuminates during the measurement interval indicating a measurement in progress.
(2)	Power ON Switch	A slide switch enabling primary power to the instrument's circuitry in the ON position.
(3)	INPUT A Connector	A BNC type connector which accepts the start input signal in the TIM modes or the input signal in the PERIOD modes.
(4)	X1, X10, X100 Multiplier Switch	A three position slide switch selecting the input multiplier for the START LEVEL control.
(5)	SLOPE Switch	A slide switch selecting either the positive (+) or negative (-) slope of the input waveform for triggering.
(6)	START LEVEL Control	A potentiometer which adjusts the input trigger level voltage between -1 volt and +1 volt times the multipler switch setting.
(7)	Display	Eight numerical indicator tubes with automatically positioned decimal point. In the X1000 mode only six tubes are used, the two least significant digits are blanked. The display reads directly in microseconds.

TABLE 2-6 (Continued)

INDEX	NOMENCLATURE	
(8)	DISPLAY TIME Control	A combined potentiometer and switch which varies the display time interval between 0.1 seconds (ccw) and 10 seconds (cw). In the extreme clockwise position a switch is activated which provides infinite display time until manual or remote reset is effected.
(9)	RESET Switch	A momentary pushbutton switch effecting instrument reset to zero when depressed.
(10)	STOP LEVEL Control	A potentiometer which adjusts the stop input trigger level voltage between -1 volt and +1 volt times the multiplier switch setting.
(11)	SLOPE Switch	A slide switch selecting either a positive (+) or negative (-) slope of the stop input waveform for triggering.
(12)	MODE - MODE X1000 Switch	A four position rotary switch selecting either the TIME INT. or PERIOD functions in either the normal (X1) or expanded (X1000) operating modes. In the expanded modes the least two digits of the visual display are blanked provided a six digit display.
(13)	X1, X10, X100 Multipler Switch	A three position slide switch selecting the input multiplier for the STOP LEVEL Control.
(14)	INPUT B Connector	A BNC type connector which accepts the stop input signal in the TIME INT. modes.

2.7 REAR PANEL DESCRIPTION

Table 2-7 and Figure 2-4 describe the rear panel controls and functions. The left hand index column is referenced to the rear panel illustration on page 2-14.

TABLE 2-7

REAR PANEL DESCRIPTION

INDEX	NOMENCLATURE	FUNCTION
(1)	REM. RESET Connector	A subminiature RF connector providing a means of resetting the instrument from a remote signal. A positive going pulse from ground to between +3 and +10 volts amplitude and greater than 1 μs duration is required. Maximum recycle rate is limited to 20 kHz.
(2)	START MARKER Connector	A subminiature RF connector providing a 150 mV (peak), 10 ns (nominal) pulse at the start triggering point. In the PERIOD functions, two pulses will be generated indicating the start and stop triggering points respectively.
(3)	STOP MARKER Connector	A subminiature RF connector providing a 150 mV (peak), 10 ns (nominal) pulse at the stop triggering point. In the PERIOD functions, no pulse appears on the STOP MARKER.
(4)	INT. - EXT. Switch	A slide switch permitting instrument operation from the internal oscillator in the INT. position or from an external 1 MHz reference in the EXT. position.

TABLE 2-7 (Continued)

INDEX	NOMENCLATURE	FUNCTION
(5)	INPUT/MON. Connector	A BNC connector providing a means of monitoring the internal oscillator when the INT. - EXT. switch is in the INT. position. When the INT. - EXT. switch is in the EXT. psoition, this connector serves as the input for the external frequency standard.
(6)	115/230 Line Switch	A recessed slide switch permitting operation from either a 115 or 230 volt ac source (refer to paragraph 2.3).
(7)	1A Fuse Receptacle	The primary power fuse holder containing a 1 ampere SLO-BLO type fuse (115 volt operation). When operating from a 230 volt source, the fuse should be replaced with a 0.5 ampere SLO-BLO type fuse to adequately protect the instrument.
(8)	Line Cord	A six foot tri-conductor cable providing a means of supplying ac power to the instrument and terminated with a molded NEMA type male connector that automatically grounds the instrument chassis when connected to a grounded power receptacle.

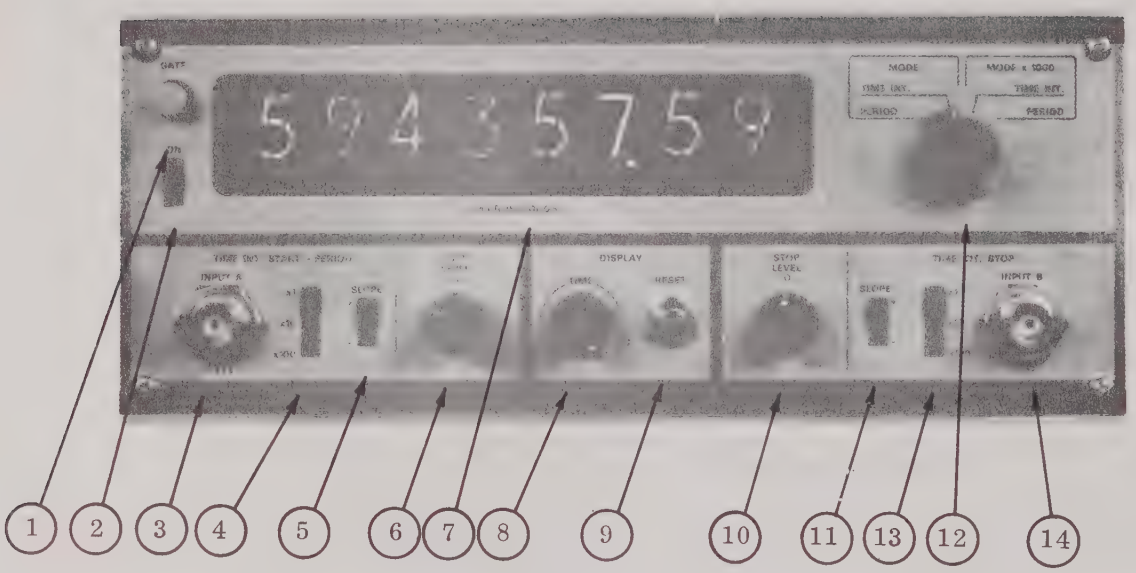


FIGURE 2-3

FRONT PANEL

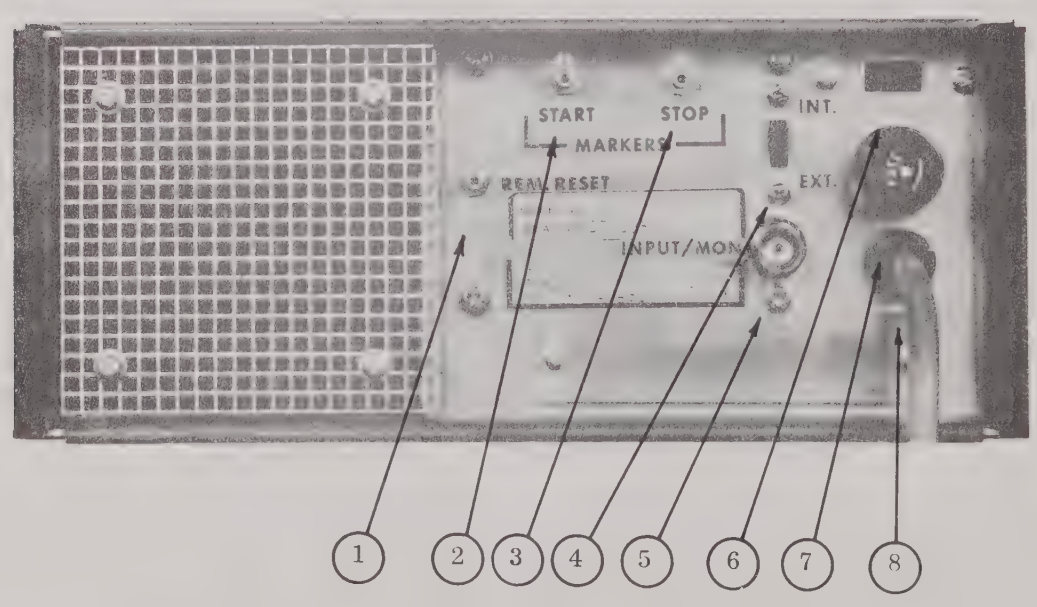


FIGURE 2-4

REAR PANEL

2.8 OPERATION

This section describes basic operational procedures for time interval, period, pulse width and rise time measurements. It is assumed that the instrument is connected to the proper source and that the power ON switch is in the ON position.

2.8.1 Time Interval Measurements

A time interval measurement is the elapsed time between an event at the INPUT A (Start) connector and an event at the INPUT B (Stop) connector. Table 2-8 describes a normal time interval measurement.

TABLE 2-8
TIME INTERVAL MEASUREMENT

STEP	ACTION
1	Insure that the rear panel INT - EXT switch is in the INT position.
2	Rotate the MODE - MODE X1000 switch to the TIME INT (X1) position and rotate the DISPLAY control to minimum (0.1 s).
3	Set the START and STOP SLOPE switches to the desired slopes for triggering.
4	Set the START and STOP multiplier switches for the appropriate input signal amplitudes.
5	Set the START and STOP LEVEL controls to maximum (fully clockwise for "+" slopes or fully counterclockwise for "-" slopes).
6	Depress the RESET pushbutton switch to clear the display and apply a series of start pulses to the INPUT A connector.
7	Gradually reduce the START LEVEL control setting until the GATE lamp illuminates.
8	Connect the stop signal to the INPUT B connector and apply a series of stop pulses.

TABLE 2-8 (Continued)

9	Gradually reduce the STOP LEVEL control setting until the GATE lamp extinguishes. The display will indicate the interval of time between consecutive start and stop pulses. If greater resolution is desired, rotate the MODE - MODE X1000 switch to the TIME INT. X1000 position. NOTE In the expanded (X1000) modes, 1000 start - stop sequences must occur before the readout is updated. As an example, a start - stop repetition rate of 100 Hz requires 10 milliseconds times 1000 or 10 seconds before the measurement can be completed and the display updated.
10	The rear panel START and STOP MARKERS can be employed in conjunction with a dual trace oscilloscope to locate the triggering points at any desired position on the input waveform. Monitor the input waveform on one trace and the START or STOP MARKER on the other trace. By superimposing the two waveforms, the point on the input waveform at which triggering occurs can be determined and readily adjusted by either the START or STOP LEVEL control.

2.8.2 Period Measurements

A period measurement is the interval of time of one complete cycle of input. In this mode the maximum input frequency is limited to 20 MHz (50 ns). Only the INPUT A circuitry is used and both start and stop pulses occur at exactly the same triggering point on the same slope. Table 2-9 outlines a basic period measurement.

TABLE 2-9
PERIOD MEASUREMENT

STEP	ACTION
1	Rotate the MODE - MODE X1000 switch to the PERIOD (X1) position and rotate the DISPLAY control to minimum (0.1 s).
2	Select the desired slope for triggering with the START SLOPE switch.
3	Set the START multiplier switch for the appropriate input signal amplitude.

TABLE 2-9 (Continued)

4	Set the START LEVEL control to maximum (fully clockwise for "+" slopes or fully counterclockwise for "-" slopes).
5	Depress the RESET pushbutton switch to clear the display and apply the input signal to the INPUT A connector.
6	Gradually reduce the START LEVEL control setting until a solution is displayed.
7	If increased resolution is required, rotate the MODE - MODE X1000 switch to the PERIOD X1000 position.
8	To trigger at a point where the waveform crosses zero, first disconnect the input, select the PERIOD (X1) mode and then rotate the START LEVEL control fully clockwise if the SLOPE switch is in the "+" position or fully counterclockwise if in the "-" position. Depress the RESET pushbutton and adjust the START LEVEL control until the GATE lamp just illuminates. This establishes a zero triggering point. Reconnect the input signal to the INPUT A connector.

2.8.3 Pulse Width Measurements

To measure the duration of a pulse the START and STOP inputs must be externally paralleled. This can be readily accomplished by means of a BNC tee type connector and additional length of cable. Table 2-10 outlines a pulse width measurement.

TABLE 2-10

PULSE WIDTH MEASUREMENT

STEP	ACTION
1	Rotate the MODE - MODE X1000 switch to the TIME INT. (X1) position and rotate the DISPLAY control to minimum (0.1 s).
2	Set the START SLOPE switch to the desired triggering slope and set the STOP SLOPE switch to the opposite position.
3	Set the START and STOP multiplier switches for the appropriate input signal amplitude.

TABLE 2-10 (Continued)

	Connect the input signal to both the INPUT A and INPUT B connector using a BNC tee and additional length of cable.
	NOTE As an additional length of coaxial cable will exhibit a fixed delay (≈1 ns per 8 inches of length), use as short a cable as possible or one of known electrical length. Subsection 2.8.5 outlines a method of determining electrical cable length using the Model 784 Time Interval Counter.
5	Using a dual trace oscilloscope, monitor the input signal and rear panel START MARKER simultaneously.
6	Adjust the START LEVEL control to locate the triggering point at the desired percentile.
7	Monitor the input signal and STOP MARKER simultaneously. Using the STOP LEVEL control, locate the triggering point at precisely the same position on the opposite slope of the input signal.
8	The display will indicate the duration of the pulse directly in microseconds. If greater resolution is desired, select the TIME INT. X1000 position of the MODE - MODE X1000 switch.

2.8.4 Rise Time Measurements

Rise time measurements are similar to pulse width measurements previously described. The SLOPE switches are, however, always placed in the identical position. Using the START and a STOP MARKERS, locate the triggering points at the desired position on the selected slope of the input waveform.

2.8.5 Cable Length Measurements

To measure the electrical length of a cable using the Model 784, follow the steps outlined in Table 2-11. The cable must exhibit an electrical length in excess of 10 nanoseconds for a valid reading.

TABLE 2-11

CABLE LENGTH MEASUREMENT

STEP	ACTION
1	Rotate the MODE - MODE X1000 switch to the TIME INT. (X1) position and place the START and STOP multiplier switches to the X1 position.
2	Place both START and STOP SLOPE switches to "+" and rotate the START and STOP LEVEL controls fully clockwise.
3	Depress the RESET pushbutton switch and adjust the START LEVEL control until the GATE lamp just illuminates (zero start triggering point).
4	Adjust the STOP LEVEL control just until the GATE lamp extinguishes (zero stop triggering point).
5	Connect a BNC tee connector to the INPUT A connector.
6	Connect the cable to measured between the tee and the INPUT B connector.
7	Apply a sine wave of less than 20 MHz to the paralleled inputs.
8	Rotate the MODE - MODE X1000 switch to the TIME INT. X1000 position.
9	The electrical length of the cable will be displayed directly in micro-seconds with 1 nanosecond resolution.

SECTION 3
THEORY OF OPERATION

SECTION 3
THEORY OF OPERATION

3.1 INTRODUCTION

This section describes and explains the theory of operation of the Eldorado Model 784 Time Interval Counter. The theory is first presented as a block diagram analysis which offers insight into basic instrument operation. A detailed description at the circuit level follows, providing the reader with a comprehensive understanding of the individual circuits which constitute the Model 784 Time Interval Counter.

3.2 BLOCK DIAGRAM ANALYSIS

The simplified block diagram for the Model 784 is illustrated in Figure 3-1. The instrument employs a 100 MHz clock signal which is gated to the 1st decade counting unit (DCU) during the measurement interval. In the time interval mode (TIM), the gated 100 MHz clock is enabled by the first start pulse and disabled by the first stop pulse resulting in the display of the time interval between pulses with 10 nanosecond resolution. The period mode, employs the start channel exclusively; the first pulse start input enables the 100 MHz clock while the second pulse at the start input disables the clock, stopping the measurement.

During operation utilizing the expanded (X1000) measurement modes, a "X999" counter is enabled requiring 1000 start-stop sequences before a measurement is completed and the solution displayed. In the expanded modes, the two least significant digits of the count chain are blanked and the decimal location is shifted three positions providing 1 nanosecond (effective) resolution.

3.2.1 Input Attenuators

The Input A (Start) and Input B (Stop) attenuators are identical and operate in conjunction with the front panel X1-X10-X100 switches. In the X1 position the input is coupled directly into the input shaper circuitry while in the X10 and X100 positions, resistive networks are inserted ahead of the shaper circuits reducing the input amplitude 10 and 100 times respectively.

3.2.2 Input Discriminator Circuits

The Input Discriminator circuits process the input signals for logic level compatibility. Individual Slope and Level controls are provided for both the start and stop channels permitting operator selection of the desired triggering level and slope.

In the Period modes, the output from the Input A (Start) channel is common to both the Start and Stop outputs providing period measurement functions.

3.2.3 Steering Logic and Gate Circuit

The steering logic and gate circuit comprise the basic timing and control functions of the Model 784. High speed ECL logic provides for the gating of the 100 MHz clock from the VCO, to the 1st DCU. The clock is gated on by the first start pulse from A discriminator. In the time interval mode (TIM) the clock is gated off by the first stop pulse from B discriminator. When operating in the period mode, the clock is gated off by the second pulse from A discriminator. When expanded mode (X1K) is selected the X999 counter is enabled allowing 1000 successive start-stop sequences before completion of a measurement period. An "end of count" (EOC) signal is generated on the completion of a measurement period and sent to the display and reset circuits.

3.2.4 Times 999 Counter

The X999 counter is enabled by the steering logic only when the expanded modes are selected. The counter consists of divide-by-ten circuit and a series of flip-flops arranged to provide a true output after 999 stop indications have been totalized. The true state output, in turn, enables a flip-flop which will be toggled by the next (1000th) stop indication, generating an end-of-count signal to the display and reset circuitry.

3.2.5 100 MHz VCO

The gated 100 MHz clock signal originates from a basic free-running oscillator. The output frequency is compared to the internal 1 MHz frequency standard and fed back to the free running oscillator forming a VCO (voltage controlled oscillator), maintaining a precise 100 MHz output frequency.

3.2.6 1st DCU

The first DCU accepts the gated 100 MHz signal from the steering logic and gate circuit. This decade consists of four high speed ECL (Emitter-Coupled Logic) flip-flops arranged to provide a divide-by-ten function to the next decade of the count chain and 1-2-4-8

binary coded decimal (BCD) information to its associated storage circuitry.

3.2.7 Count Chain

The count chain consists of the seven remaining DCU's and their associated storage, decade and display circuits. The 10 MHz output from the 1st DCU is directly coupled to the first decade (2nd DCU) of the count chain. Each decade receives the divide-by-ten output from the previous decade and provides 1-2-4-8 BCD information to its associated storage circuit. At the conclusion of the measurement interval, the contents of the storage registers are enabled to the decoding circuits providing a visual display of the accumulated count.

3.2.8 Display and Reset Circuit

The display and reset circuit receives the "end of count" signal from the steering logic and gate circuitry and, in turn, generates the storage transfer pulse to the storage registers. The end of count pulse also enables the display timer which determines the display interval. At the conclusion of the display interval, a reset pulse is generated which resets the count chain, X999 counter and the steering logic and gate circuitry, preparing the instrument for a succeeding measurement.

3.2.9 BCD Data Output Option P1

The P1 option circuit provides output BCD data and print command to a rear panel connector. The data is buffered and converted to 1-2-4-8 positive true positive zone logic.

3.3 CIRCUIT ANALYSIS

This section approaches the theory of operation from a detailed circuit description. The figure number included with the subsection title block refers to individual schematic located in Section 6 of this manual.

3.3.1 Input Attenuators (Figure 6-1)

Since the Input A (Start) and Input B (Stop) attenuators are identical, the following discussion will focus only on the Input A (Start) attenuator.

The input signal is coaxial cabled from Input A (Start) connector J1 to Input attenuator switch S3. In the X1 position, the signal will be coupled across the switch contacts

and, in turn, coaxial cabled to pad 27, the input to the discriminator circuit. In the X10 position, the resistive network consisting of R1, R2 and R3 is inserted into the circuit, decreasing in the input amplitude by a factor of 10. In the times 100 position, resistors R4 and R5 are added to the resistive network, effectively reducing the input signal amplitude 100 times in magnitude.

3.3.2 Input Discriminator Circuits (Figure 6-1)

The input shaper circuits convert input signals into positive going pulses compatible with the ECL Start-Stop flip-flop of the steering logic and gate circuit. As both the Input A (Start) and Input B (Stop) discriminators are identical, the detailed description is referenced to the Input A (Start) discriminator exclusively.

The input discriminator consists of two differential amplifiers, a tunnel diode pulse generator and an output buffer circuit. The differential amplifiers provide an output which is representative of the input voltage. When this output is of sufficient magnitude, the tunnel diode will rapidly change to its high voltage state. The diode level change is differentiated into a pulse which is, in turn, coupled to the output buffer where it is brought to the proper logic levels.

The output from the attenuator is coupled to the cathode of diode CR1. A positive going pulse will reverse bias diode CR1 enabling a positive potential to the base of differential transistor Q1 through R8 and CR2. A negative going pulse will be coupled through CR1, reverse biasing diode CR2, enabling a negative potential to the base of Q1 through R9. The input signal amplitude required to cause the tunnel diode to switch to its high voltage state is determined by the position of front panel LEVEL control R17. The collectors of transistors Q1 and Q2 (1st differential) are coupled to the bases of transistors Q3 and Q4 (2nd differential) respectively. A positive pulse will decrease the conduction of transistor Q1 which increases the conduction of transistor Q2. This action increases the conduction of Q3 while decreasing the conduction of Q4, causing the differential output at the collector of Q4 to become more positive. A corresponding negative pulse at the input will increase the conduction of transistor Q4 causing the differential output to become more negative.

The tunnel diode pulse generator is directly coupled to the collector of Q4. In a quiescent state, tunnel diode CR5 is biased to its low voltage state by slope switch S5. Selecting positive (+) slope forward biases transistor Q5, grounding the cathode of the tunnel diode completing the circuit from ground, through the tunnel diode, diode CR4, R23 and R24 to the +4.9 volt potential at the slope switch. Placing slope switch S5 in

the negative (-) position forward biases transistor Q6, grounding the anode of the tunnel diode. This completes the circuit from the -4.9 volt potential, through R23, R24, CR3 and the tunnel diode to ground.

The tunnel diode, remains in its low voltage state until the differential output at the collector of Q4 supplies sufficient current to switch the diode to its high voltage state. This occurs when the input amplitude corresponding to the selected slope exceeds the level control setting. The tunnel diode quickly changes state generating a positive going step which is differentiated into a positive going pulse by the LR network comprised of L3 and R26.

Transformer T1, in turn, couples a negative going pulse to the base of emitter follower Q7, momentarily reverse biasing the transistor. Capacitor C5 couples a negative pulse to the base of Q8, forward biasing the transistor, bringing the start output up from a -4.9 volt level towards ground, generating a start pulse to the start-stop flip of the steering logic and gate circuit.

Potentiometer R24, in the trigger diode pulse generator circuit, is a symetry adjustment. This potentiometer is employed to set the triggering point at the same level on both the positive and negative slope. Transformer T2, on the start output, couples a positive going pulse from ground to approximately 150 mV to the rear panel start marker connector whenever a pulse is generated from the Input A (Start) discriminator. This pulse can be used to locate the desired triggering point on the input waveform.

3.3.3 Steering Logic and Gate (Figure 6-2)

The steering logic and gate circuitry incorporates high speed emitter-coupled logic (ECL) to gate the 100 MHz clock signal from the VCO into the 1st DCU. Due to the complexity of the logic involved, each mode of operation will be discussed separately.

3.3.3.1 Time Internal Mode

In the time interval mode (TIM) the 100 MHz clock is essentially enabled by the first start pulse from the Input A discriminator and disabled by the first stop pulse from the Input B discriminator. The discriminator outputs are coupled directly to start stop flip-flop MC1. Selecting the TIM mode grounds (logic high state) the TIM line through mode switch S7B. This causes the outputs from NOR gates MC12B and MC10A to assume low states. The output from MC12B enables the stop input to MC1 while the out-

put from MC10A enables end-of-count flip-flop MC4. The start input to MC1 is enabled approximately 25 μs following MECL reset by the hold off circuit consisting of MC2A, MC2B and MC2C. This assures that the count chain will be clear and that all logic will be in its initial state prior to the recognition of a start pulse.

A positive going state pulse from the discriminator toggles the Q output of MC1 to a low state and the $\overline{Q}$ output to a high state. The Q and $\overline{Q}$ outputs from MC1 are coupled to synchronous flip-flop MC9. The flip-flop is, in turn, toggled by the non-inverted 100 MHz clock signal from MC3A, delayed 5 to 7 ns by coax delay line D7 which is cut to equal the propagation delay of MC9, causing the Q output from MC9 to assume a low state. The low state output enables MC3B, coupling the inverted 100 MHz clock from MC3A to the 1st DCU. Opening the gate coincident with the clock signal rather than the actual start pulse prevents a -1 count gating error. The counting circuitry totalizes the 100 MHz clock signal for the duration that NOR gate MC3B is enabled. A stop pulse at the $\overline{J}$ input to MC1 toggles the flip-flop, changing the state of the Q and $\overline{Q}$ outputs. The ensuing negative transition of the 100 MHz clock signal toggles the synchronous flip-flop, causing the Q output to assume a logic high state. The high state output disables the 100 MHz clock at NOR gate MC3B and toggles the end of count flip-flop MC4, causing the $\overline{Q}$ output to assume a high state. The high state $\overline{Q}$ output is coupled through logic translator MC13A providing the end of count indication to the display and reset circuitry and through the non-inverted output of MC12A, setting the start-stop and synchronous flip-flops to their initial states.

3.3.3.2 Period Mode

Operation in the period (X1) mode is identical to the time interval mode described in sub-section 3.3.3.1. The stop pulse to start-stop flip-flop MC1 originates from the Input A (start) discriminator. Mode switch S7A (Figure 6-1) connects the Input A discriminator output to both the start and stop inputs of flip-flop MC1. The first pulse initiates the measurement and the second pulse stops the measurement.

3.3.3.3 Time Interval X1000 Mode

In the TIM X1000 mode, 1000 start-stop sequences are required before end of count flip-flop MC4 is toggled, generating the end-of-count indication to the display and reset circuitry. Selecting the TIM X1000 mode grounds (logic high state) the TIM' line into the steering logic. This results in a low state output from MC12B, enabling the stop input to MC1. The high state TIM' line also disables NOR gate MC10D, preventing recognition of stop pulses from NOR gate MC10C into X999 flip-flop MC11. Since the

Period X1000 mode is not selected, the P' line into the steering logic will maintain a logic low state through resistor R72. The low state at NOR gate MC2D enables the $\overline{Q}$ output from synchronous flip-flop MC9 to the $\overline{J}$ and $\overline{K}$ input of X999 flip-flop MC11. At the conclusion of each time interval measurement sequence, the $\overline{Q}$ output from MC9 will be low causing a high state output from MC2D, toggling the X999 flip-flop. The $\overline{Q}$ output from MC11 is coupled through logic level converter MC13B into the remainder of the X999 counter.

After 999 stop indications have been totalized into the X999 counter, the counter output at MC15A will be low. This low state output is, in turn, coupled to NOR gate MC10B. The remaining input to MC10B is the Q output from the X999 flip-flop. Originally set to a high state output by the MECL reset pulse, the Q output will be low on odd numbered counts. On the 999th count, both inputs to NOR gate MC10B will be low producing a high state output. This output is coupled to NOR gate MC10A resulting in a low state output which enables end of count flip-flop MC4. At the conclusion of the 1000th measurement, the Q output from synchronous flip-flop MC9 returns to a high state, toggling the end of count flip-flop, providing the end-of-count indication to the display and reset circuit.

3.3.3.4 Period X1000 Mode

In the Period X1000 mode a measurement is initiated by the first pulse at the start input and allowed to continue until 1000 additional pulses have been received from the Input A discriminator. Selecting the Period X1000 mode grounds the P' line into the steering logic while the remaining mode lines are held to a low state. The high state P' line disables NOR gate MC2D, blocking the $\overline{Q}$ output from MC9 to X999 flip-flop MC11. Recalling that the output from NOR gate MC10B is low until the count of 999, the output from 4 input NOR gate MC12B will be at a high state, disabling the $\overline{J}$ (stop) input to start-stop flip-flop MC1. The first input pulse causes the Q output from synchronous flip-flop MC9 to assume a low state, enabling the 100 MHz gate (MC3B) and NOR gate MC10C. Consequent input pulses cannot toggle the start-stop flip-flop since the output from MC12B is high. These pulses are, however, coupled through enabled NOR gate MC10C and, since the TIM' line is low, through NOR gate MC10D to X999 flip-flop MC11. The X999 counter now counts the number of input pulses rather than $\overline{Q}$ output transitions from MC9. After 999 input pulses have been totalized, the output from the counter at MC15A assumes a low state. As in the TIM X1000 mode, both inputs to NOR gate MC10B will now be low resulting in a high state output. The high state output,

in turn, results in low state outputs from MC12B and MC10A enabling the $\overline{J}$ (stop) input to MC1 and end-of-count flip-flop MC4 respectively. The next input pulse toggles start-stop flip-flop MC1, enabling synchronous flip-flop MC9. The next negative transition of the 100 MHz clock from MC3A toggles the synchronous flip-flop, disabling the 100 MHz gate and toggling end of count flip-flop MC4.

3.3.4 X999 Counter (Figure 6-2)

The X999 counter is enabled only during operation in the X1000 (expanded) modes. In the TIM X1000 mode, X999 flip-flop MC11 is toggled by the $\overline{Q}$ output from synchronous flip-flop MC9 while in the Period X1000 mode, the flip-flop is toggled by input pulses at the stop input to start-stop flip-flop MC1. The $\overline{Q}$ output (divided-by-two) from MC11 is coupled to decade counter MC16 through logic translator MC13B. The divided-by-ten output from MC16 is coupled to flip-flop MC17, the first in a series of six flip-flops. The counting logic is arranged so that on the count of 999 the $\overline{Q}$ output from MC19 will be low, reverse biasing transistor Q18 while the outputs from NOR gates MC20B and MC20D will both be at a logic high state. This enables the positive potential through R76 to the base of transistor Q17, forward biasing the transistor, grounding (logic low state) it's collector. The low state at the collector of Q17 is directly coupled to logic translator MC15A which results in an ECL low state output to MC10B. Since the Q output from the X999 flip-flop is low on the count of 999, the output from MC10B will be at a high state resulting in a low state output from MC10A, enabling end of count flip-flop MC4.

3.3.5 100 MHz VCO (Figure 6-4)

The 100 MHz VCO (voltage controlled oscillator) consists of a 100 MHz oscillator which is located on the underside of the main pc board and a phase lock circuit. The 100 MHz oscillator is essentially a free running oscillator with complementary outputs. One output (output A) is coupled to the steering logic and gate circuitry as the 100 MHz clock signal while the other output (Output B) is coupled into the phase lock circuit.

The 100 MHz output (Output B) at the emitter of Q1 is capacitively coupled to the toggle inputs of J-K flip-flop MC21. Flip-flops MC21, 22, 23 and 24 are arranged to provide a divide-by-ten function at the output of logic converter MC14D. This output, now 10 MHz, is coupled to the input of decade counter MC27. The resultant 1 MHz output, at pin 12, is coupled to the toggle input of flip-flop MC26A. The 1 MHz reference from the internal oscillator is inverted at NOR gate MC25D and coupled to flip-flop MC26B.

The Q output from MC26A is coupled to enabled NOR gate MC25A while the $\overline{Q}$ output from MC26B is coupled to enabled NOR gate MC25C.

The outputs from these NOR gates are differentiated into triangular waveforms by RC networks (C36-R130 and C39-R131) and summed at the junction of resistors R132 and R133. The resultant signal is coupled back to the 100 MHz oscillator. The LC network comprised of L2, C1, C8 and C10 filters the signal to a dc level which is coupled to the junction of varicap diodes CR1 and CR2.

When the divided 100 MHz signal and 1 MHz reference signal are exactly in phase, flip-flops MC26A and MC26B will be toggled simultaneously. This causes the Q output of each flip-flop to assume a logic high state while the corresponding $\overline{Q}$ outputs will be low. The $\overline{Q}$ outputs from each flip-flop are directly coupled to NOR gate MC25B. With both inputs low, the output from MC25B will be high, clearing both flip-flops. When cleared, the low state Q output from MC26A will be inverted by MC25A and differentiated by R130 and C36 resulting in a positive going level shift at R132. The high state $\overline{Q}$ output from MC26B will be inverted by MC25C and differentiated by R131 and C39 resulting in a negative going level shift at R133. Since the level shifts are in direct opposition, the resultant output at the junction between R132 and R133 will be the average between the two levels (approximately +1.8 volts).

When the divided 100 MHz signal leads the 1 MHz reference signal, flip-flop MC26A will be set before flip-flop MC26B is set. During the interval after MC26A is set and before MC36B is set, the Q output from MC26A will be at a logic high state as will the $\overline{Q}$ output from MC26B. Both the output from MC25A and from MC25C will consequently, assume low states, causing a negative level shift at the sum junction between R132 and R133. The negative dc level shift at the junction of diodes CR1 and CR2 will cause a corresponding increase in their capacitance. An increase in capacitance, in turn, will decrease the 100 MHz oscillator's output frequency. The ensuing negative transition of the internal 1 MHz reference signal toggles flip-flop MC26B. The $\overline{Q}$ output from MC26B will assume a low state output, causing the output from MC26B to be high, clearing flip-flops MC26A and MC26B.

Similarly, if the 1 MHz reference pulse leads the divided 100 MHz oscillator pulse, MC26B will be set before MC26A. When this occurs, the Q output from MC26A will be low as will the $\overline{Q}$ output from MC26B. NOR gates MC25A and MC25C will both exhibit

a positive going level shift which, at diodes CR1 and CR2, will cause a decrease in capacitance, increasing the 100 MHz oscillator's output frequency.

3.3.6 1st DCU (Figure 6-2)

The 1st DCU incorporates four high speed emitter coupled logic flip-flops, a storage register, decimal decoder and corresponding numerical readout tube. The 100 MHz clock signal from the 100 MHz gate is directly coupled to the toggle inputs of flip-flop MC5. Flip-flops MC5, 6, 7 and 8 are arranged to provide 1-2-4-8 BCD outputs to storage register MC30 and a divided-by-ten (10 MHz) output from logic converter MC13D to the next decade (10^1) of the count chain. Since the storage register employs resistor-transistor logic (RTL), logic converters MC14A, MC14B, MC14C and MC13C are added to convert the 1-2-4-8 flip-flop outputs to the proper logic levels.

After a measurement is completed, the contents of the storage register are enabled to decimal decoder MC31 by the storage transfer pulse. MC31 translates the 1-2-4-8 data into ten line decimal information, enabling the corresponding digit within numerical indicator tube V1.

During operation in the expanded (X1000) operating modes, the numerical indicator tubes representing the two least significant digits of the display (1st and 2nd DCU's) are blanked. Selecting either the TIM X1000 or Period X1000 modes grounds the anode of diode CR15 through mode switch S7C, forward biasing transistors Q19 and Q20. Forward biasing the transistors shunts the +230 volt indicator tube plate supply through neon lamps DS1 and DS2 to ground, darkening numerical indicator tubes V1 and V2.

The 1st DCU also controls the gate lamp, indicating a measurement in progress. The Q output of flip-flop MC7 is originally set to a high state by the MECL reset pulse. On the count of 4, the Q output assumes a logic low state resulting in an RTL low state output which toggles the gate flip-flop in the display and reset circuitry, illuminating the front panel gate lamp.

3.3.7 Count Chain (Figure 6-3)

The count chain includes the remaining decades with their associated storage registers, decimal decoders and numerical indicator tubes. The 10 MHz signal from the 1st DCU is coupled to the input of decade counter MC32. MC32, in turn, provides a 1-2-4-8

count output to MC33 and a divided-by-ten output which is inverted by MC28A and coupled to the input of decade counter MC35. Each succeeding decade counter provides a 1-2-4-8 count output to its associated storage register and a divided-by-ten output to the next decade. The contents of the storage registers are enabled to their corresponding decimal decoders by the storage-transfer pulse generated at the conclusion of the measurement interval.

Decimal point location is determined by the MODE switch position. In the normal modes, switch S7C grounds the DEC. 3 line enabling the decimal point within numerical indicator tube V3 while in the expanded modes, switch S7C grounds the DEC. 6 line enabling the decimal point within indicator tube V6.

3.3.8 Display and Reset Circuit (Figure 6-3)

The display and reset circuit accepts the end-of-count indication from the steering logic and gate circuitry and, in turn, generates the storage transfer and RTL reset pulses. The positive going end-of-count level shift triggers the storage one-shot causing a low state output from MC28B. Capacitor C30 couples a negative pulse to the input of enabled NOR gate MC28D, producing a high state output which forward biases transistor Q25, generating the negative going storage-transfer pulse. The RC time constant of C30 and R114 fixes the pulse width at approximately 5 μs. The positive going output pulse from MC26D also clears gate flip-flop MC53, reverse biasing transistor Q26, extinguishing the GATE lamp.

The high level end-of-count indication produces a low state output from MC28C, enabling the display timer. The low state output forward biases transistor Q27 resulting in a positive potential at its collector. This positive potential will charge capacitor C34 as long as INF switch S8 remains in the NORM position. The charging rate is determined by the RC time constant of C34 and display potentiometer R106 and ranges from approximately 0.1 seconds to 10 seconds. When the charge across the capacitor reaches the conduction level of unijunction transistor Q28, the transistor conducts coupling a positive transition across capacitor C27 to enabled NOR gate MC29A.

This produces a negative going pulse at the output of MC29A which is coupled across capacitor C28 to the base of transistor Q29. The negative pulse forward biases the transistor driving the collector positive and toggling the reset one-shot comprised of MC29B and MC29C. The positive going output from MC29C is inverted by MC29D.

The resultant negative going pulse reverse biases transistor Q30 which, in turn, forward biases transistor Q31, generating the positive going RTL reset pulse. The reset one-shot fixes the reset pulse width at approximately 35 μs. The RTL reset pulse generates the negative going TTL reset pulse at the collector of Q21. This pulse resets decade counter MC32 in the count chain and MC16 in the X999 counter. The positive going RTL reset pulse, at logic converter MC15B (Figure 6-2), produces the positive going MECL reset pulse.

3.3.9 Power Supply (Figure 6-7)

All working voltages required by the instrument are derived from a primary power source. Each individual supply is regulated against source variations with the exception of the +230 volt unregulated plate supply.

Power to the primary circuit of transformer T201 is controlled by front panel switch S201 and protected by fuse F201. The power transformer has two 115 volt primary windings. The windings are placed in series for 230 volt operation or in parallel for 115 volt operation by rear panel switch S202. The rear panel mounted fan B201 is designed to operate only on 115 volts and is connected across one of the primary windings.

Transformer T201 incorporates three separate secondary windings to develop the various levels. The unregulated +230 volt dc indicator tube plate supply is referenced to the single secondary pin 6 to ground. Capacitor C203 filters the rectified high voltage from CR208 to the required +230 volt dc level.

Full wave bridge rectifier CR209 and filter capacitors C204 and C205 reduce the 28.5V rms center taped secondary voltage to approximately ± 18 volts dc. The center tap is returned to ground thus referencing the ± 12 volt supplies to ground. Zener CR210, transistor Q210 and resistors R215 and R216 is the series regulator for the +12 volt supply. Q210 base is held at +12.6 volts, and the resultant base to emitter voltage drop places the emitter at +12 volts. Zener diode CR213 transistor Q211 and resistors R217 and R218 form a constant current source for the -12 volt supply; thus providing the base drive for transistor Q212, the -12V dc series regulator. Zener CR212 holds Q212 base voltage at -12.6 volts, and the emitter-base voltage drop places the emitter at -12 volts dc.

Full wave bridge CR201 thru CR204, and filter capacitors C201 and C202 reduce the 12V rms center taped secondary voltage to approximately ± 7 volts dc, which supply the +3.6 volt, +4.9 volt and the -4.9 volt regulated supplies. All three of the power supples are referenced to the ± 12 volt supply and are the same in basic operation.

The +3.6 volt supply is current regulated and referenced to the +12 volts supply. The voltage divider R202 and ZR205 determines the base drive of transistor Q202, which in turn, controls the base drive to series regulator Q203. A change in the output level is monitored on the emitter of Q202 and any change will, in turn, cause a subsequent change to the base of Q203 maintaining the voltage at +3.6 volts by varying the current. Q201, R201 and R203 are current limiting components and will "fold back" the supply in the event of a short or high load.

The +4.9 volt supply is current regulated and referenced to the +12 volt supply. Voltage divider R210 and CR206 determines the base drive of transistor Q205 which, in turn, controls the series regulator Q206. A change in the output level is monitored by the emitter of Q205 and any change will cause a subsequent change to the base of Q206 maintaining the output voltage at +4.9 volts by varying the current. Transistor Q204 and voltage divider R209 and R212 are current limiting components and will "fold back" the supply in event of a short or high load.

The -4.9 volt supply is current regulated and referenced to the -12 volt supply. Voltage divider R206 and ZR207 determines the base drive of transistor Q208 which, in turn, controls series regulator Q209. A change in the output level is monitored by the emitter of Q208 and any change will cause a subsequent change to the base of Q209 maintaining the output voltage at -4.9 volts by varying the load current. Transistor Q207 and voltage divider R204 and R205 are current limiting components and will "fold back" the supply in the event of a short or heavy load.

3.3.10 P1 Option Circuit (Figure 6-5)

The binary coded decimal (BCD) output option circuit provides a 40 bit parallel data output consisting of 32 bits numeric data, 4 bits decimal location data, and 4 bits legend data. The numeric data is obtained from storage registers MC30 (see figure 6-2), MC34, MC37, MC40, MC43, MC46, MC49 and MC50 (see figure 6-3) and referenced to positive true logic by 22 ohm pull-up resistors R20 thru R51, which provide digital data with logic "0" equal to 0 volts ± 0.3 volts and logic "1" equal

to +5 volts ± 0.7 volts.

The print command is generated when the end of count signal (EOC) provides a low at the base of Q3. Transistor Q3 and inverter element U1D comprises a one-shot RS multivibrator which generates a 25 μs wide positive pulse. Transistors Q1, Q2 and inverter element U1E form an output driver amplifier which provides the required drive to the remote printer, as a positive going 0 to +5 volt fast rise time pulse of 25 μs duration in pulse width.

When a (+) inhibit signal is received as a positive going step of +2.5 volts or greater, inverters U1B and U1C converts the input signal to a +5 volt step which is coupled thru C1 to the base of Q3 thus holding off the print command one-shot Q1 and U1D, inhibit release occurs when the (+) inhibit signal returns to zero volts. When a (-) inhibit signal in the form of a negative going step of 0 volts or greater is received inverter U1A converts this signal to a +5 volt step which will hold-off the print command one-shot Q3 and U1D, release of the (-) inhibit occurs when the input returns to a level of greater than ≥+1 volt.

Decimal location data is obtained from switch S7C (see figure 6-3) which provides a ground return input to inverter U2D when placed in X1 position (DEC 3) thus providing a high BCD "1" output, when S7C is placed in X1000 (DEC 6) position a ground is provided to inverter U2F providing a high "4" BCD output. The BCD "2" output is high at all times due to the grounded input of inverter U2E, and the BCD "8" output is low at all times by being directly returned to ground.

The legend BCD output is fixed in a 1000 binary format, due to the configuration of exclusive OR gates U3A, B and C. Exclusive OR gate U3B has one input open and the other grounded thus presenting the BCD "1" output as a high (logic 1), exclusive OR gates U3A and C have both inputs open thus presenting BCD bits "2" and "4" as low (logic 0) outputs, the BCD "8" output bit is grounded thus presenting a low (logic 0) output.

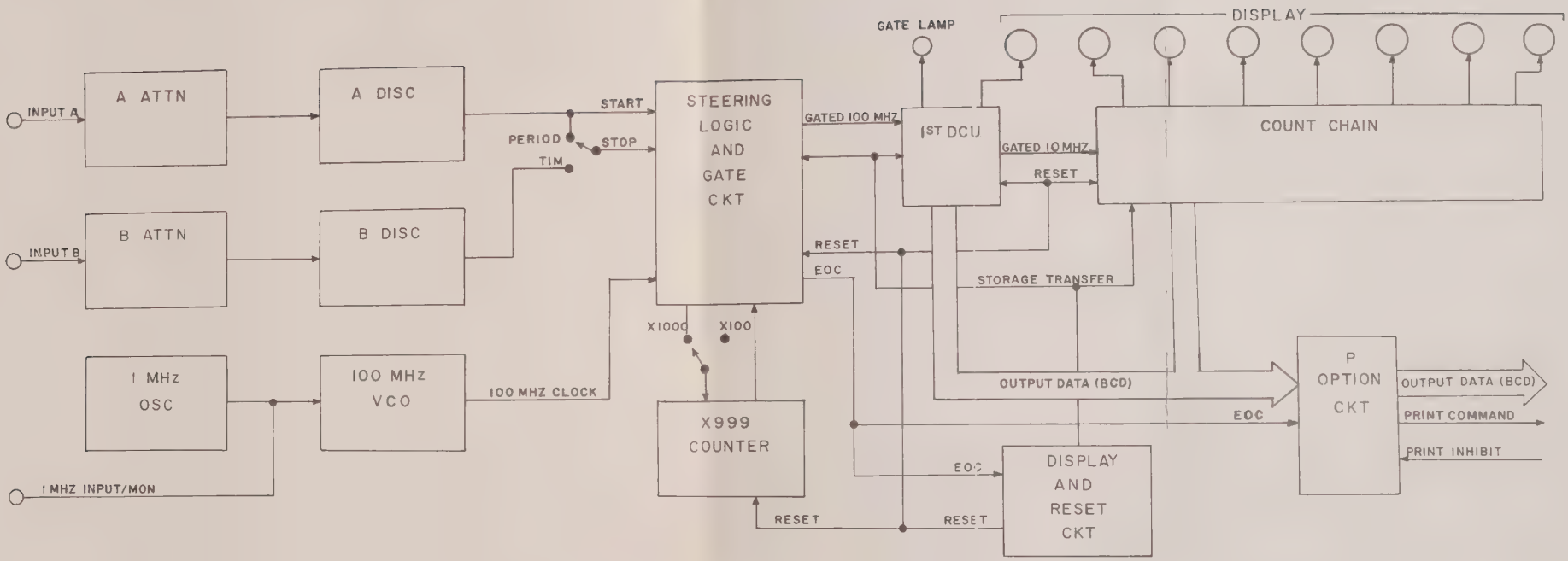


FIGURE 3-1
MODEL 784 SIMPLIFIED BLOCK DIAGRAM

SECTION 4
MAINTENANCE - CALIBRATION

SECTION 4
MAINTENANCE AND CALIBRATION

4.1 INTRODUCTION

This section presents pertinent information for maintenance of the Model 784 Time Interval Counter which includes servicing, troubleshooting, alignment, adjustment repair, and component replacement procedures. Schematic diagrams, and component location drawings are contained in section 6 of this manual in support of the maintenance procedures. Table 4-1 offers a list of suggested test equipment required for instrument calibration and repair (equivalent test equipment is acceptable).

TABLE 4-1
RECOMMENDED TEST EQUIPMENT

INSTRUMENT DESCRIPTION	MANUFACTURE AND MODEL	MINIMUM REQUIREMENTS
Oscilloscope	Tektronix 585A w/Type 82 plug-in.	80 MHz bandwidth, Dual trace.
1 MHz Frequency Standard	Any	10 times interval accuracy.
Digital Voltmeter	Eldorado Model 1820	3% accuracy
Test Oscillator	HP 651B	10 Hz to 10 MHz range
*Delay Generator	Eldorado Model 650	Selectable delays 1 ns to 1 second.
*Frequency Counter	Eldorado Model 325B	20 MHz range
**Oscilloscope	Tektronix 475	200 MHz bandwidth, Dual trace.

* Required only to verify accuracy of specifications.

** Required only for Channel Balance procedures (refer to 4.7.3)

4.2 PERIODIC MAINTENANCE

Periodic maintenance for the Model 784 Time Interval Counter is limited to routine cleaning of the fan air filter, checking the physical integrity of P.C. boards, mounts, hardware and standardization of the 1 MHz time base. Under normal operating environment, a 90 day maintenance interval is suggested.

4.3 CALIBRATION

Adjustment of the internal oscillator (time base) is the only calibration requirement of the Model 784. All other internal adjustments are factory set and are not subject to routine calibration.

4.3.1 Standardization, 1 MHz Time Base

The frequency of the internal 1 MHz oscillator may be adjusted relative to a 1 MHz frequency standard by observing rotation of a Lissajous pattern as depicted by the test configuration in figure 4-1. For optimum counter accuracy, the oscillator should be calibrated after 30 days operation due to the higher aging rate of the crystal, and at 90 day intervals thereafter. As oscillator aging is greatest when first placed into operation, instrument power should be maintained whenever possible. Table 4-1 outlines the procedure for oscillator calibration.

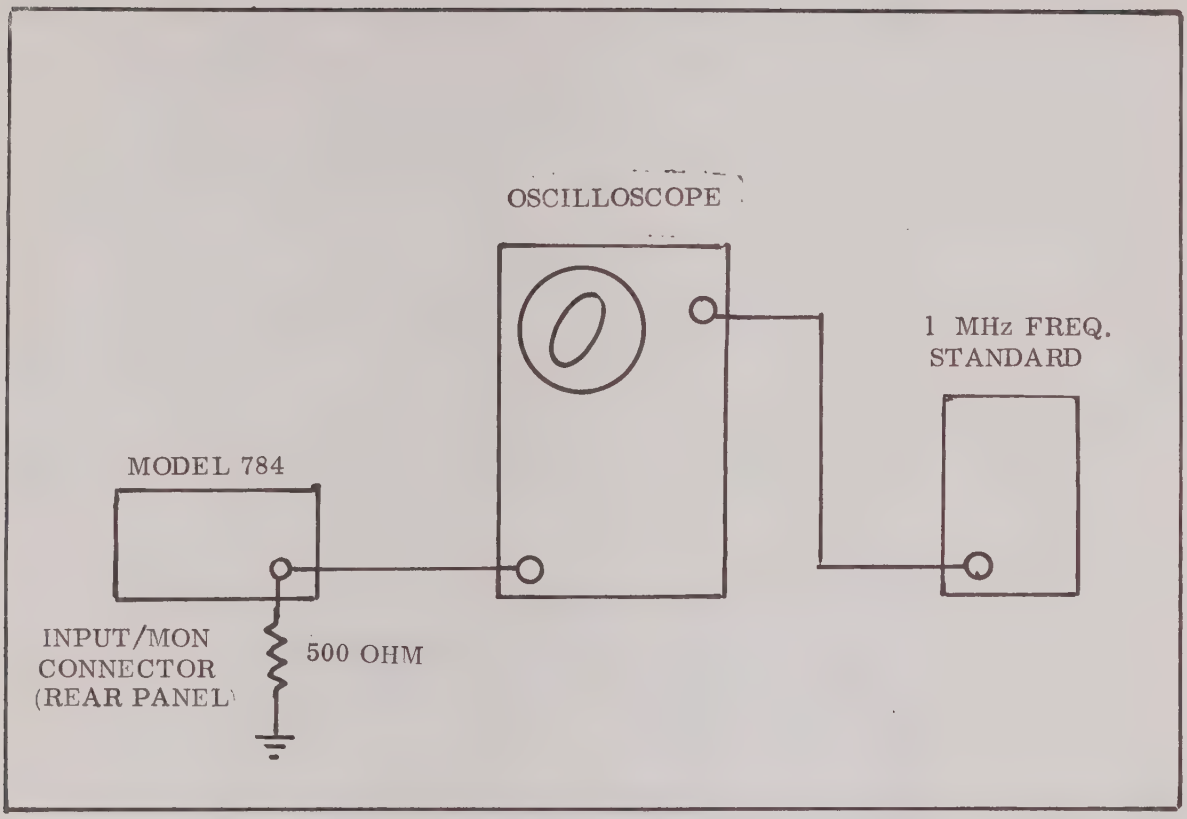


FIGURE 4-1
1 MHz TIME BASE STANDARDIZATION TEST CONFIGURATION

TABLE 4-2
TIME BASE STANDARDIZATION

STEP	ACTION
1	Apply power to instrument and allow a minimum of one hour continuous operation for oscillator stabilization.
2	Connect the oscillosceope's vertical input to the INPUT/MON BNC connector with a 500 ohm load to ground.
3	Insure that the INT/EXT switch on the rear panel of the 784 is in the INT position.

Table 4-2 Time Base Standardization (continued)

STEP	ACTION
4	Verify that the waveform swings from a minimum of 0 to +0.2 volts to a maximum in excess of +1.4 volts with a duty cycle of approximately 25%.
5	Connect the 1 MHz frequency standard to the oscilloscope's horizontal input and set the scope's horizontal input switch to external.
6	Adjust the oscilloscope for a Lissajous pattern, the pattern will be distorted due to the waveform of the 784 1 MHz.
7	Remove the top cover panel by extracting the phillips head screws securing the cover to the chassis frame.
8	While observing the Lissajous pattern adjust variable capacitor C-17 located on the top of logic display P.C. board for minimum rotation.
9	Replace top cover panel and observe the pattern for five minutes noting Lissajous ratation rate. If the rotation rate increases, remove the top cover panel and readjust capacitor C-17 for minimum rotation. Again replace the cover panel and observe the rotation rate for five minutes. Continue to monitor and adjust the oscillator until minimum rotation is realized. The cover panel must be in place as it effects both capacitance and internal temperature.
10	Disconnect test configuration and replace the cover panel. Note data for next required calibration.

4.4 INTERNAL ADJUSTMENTS

With the exception of the 1 MHz oscillator, the internal calibration adjustaments require no periodic compensation. Calibration of these "semi-fixed" adjustments is required only when a component is replaced or if a decrease in performance specifications or functional failure is apparent.

4.4.1 VCO Phaselock Adjustment

The 100 MHz VCO serves as the instruments basic reference frequency. When properly adjusted it is phaselocked to the 1 MHz reference. If phaselock is lost the piston trimmer C4 adjustment will bring the VCO into locking range of the phaselock loop. Procedure for the VCO phaselock adjustment is outlined in table 4-3.

TABLE 4-3
VCO PHASELOCK ADJUSTMENT

STEP	ACTION
1	Observe waveform at pin 9 of decade counter MC27 with a oscilloscope and reference this 10 MHz signal with the 1 MHz signal at rear panel INPUT/MON connector.
2	Adjust trimmer C4 located on the VCO auxiliary P.C. board so that the positive edge of the 1MHz signal and the negative edge of the 10 MHz signal when reference exhibits less than ≈15ns jitter.
3	Cycle power off-on switch and insure that circuit will automatically lock by observing waveform.

4.4.2 Trigger Symmetry Adjustments.

The input discriminators should trigger at the same input voltage level for either slope position. If this condition is not realized, perform trigger symmetry adjustments using test configuration as depicted in figure 4-2 and procedures outlined in table 4-4.

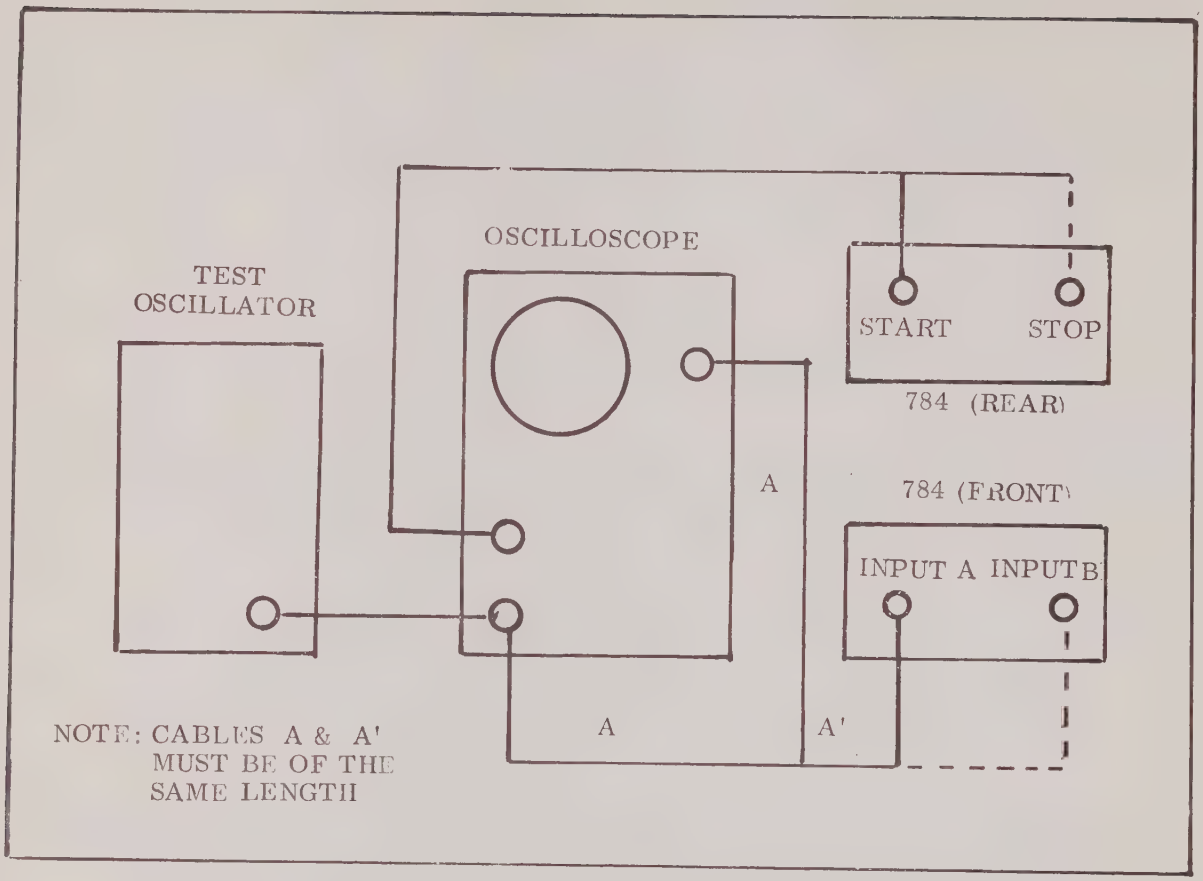


FIGURE 4-2
TRIGGER SYMMETRY ADJUSTMENTS CONFIGURATION

TABLE 4-4
TRIGGER SYMMETRY ADJUSTMENTS

STEP	ACTION
1	Place 784 mode switch in TIME INT MODE position, set A and B attenuators to X1 position.
2	Configure test equipment and cabling as shown in Figure 4-2, and adjust test oscillator for a 100 KHz 1 volt rms output.

Table 4-4: Trigger Symmetry Adjustments (continued)

3	Apply test signal to INPUT A and connect oscilloscope to MARKERS START connector.
4	With oscilloscope triggered externally by the 100 KHz test signal, display the test signal and start marker simultaneously on the oscilloscope.
5	Set 784 START LEVEL and STOP LEVEL controls for ±0.5 volts.
6	Adjust symmetry potentiometer R24 so that the onset of the marker occurs at the same input voltage level (±20 mV) on both the + and - slopes.
7	Repeat for INPUT B and STOP MARKER using symmetry potentiometer R-51.

4.5 FAULT ISOLATION

This section furnishes basic information necessary to determine the nature and location of an instrument failure.

Fault isolation is the process of isolating a fault or failure to three increasingly detailed levels. The first level of isolation is to "sectionalize" the fault to a sub-assembly, such as the power supply, display P.C. board or VCO auxiliary P.C. board. Once isolated to a sub-assembly, the second level or "localization" of the failure is undertaken to confine the fault to an individual stage, circuit or logic function within the sub-assembly. The third level of isolation involves the location of the defective component, which can be a discrete element or an IC component such as a dual in line package (DIP) IC containing a number of logic elements.

In the event of a suspected failure and before any fault isolation or repairs are attempted:

1. Insure that the A and/or B inputs being applied are of sufficient amplitude to trigger the input discriminator circuits.

2. Verify the proper positioning of all operational switches and controls.
3. Attempt resetting of the power supplies by cycling the power on-off switch.

NOTE

The instruments +3.6 volt and ±4.9 volt power supplies are provided with short circuit protection. A momentary short or a primary power surge will activate the protection circuit(s) and hold the supply off until instrument's primary power is turned off and on again.

If a valid malfunction is encountered, first insure that all DC power levels are present and correct before attempting to sectionalize the malfunction.

4.5.1 SECTIONALIZATION

Sectionalization is based on performance checks and waveform measurements; Table 4-5 outlines procedures for sectionalizing faults. The table is sequenced and should be followed in proper order.

TABLE 4-5

MODEL 784 SECTIONALIZATION AND LOCALIZATION

Are proper voltages present at emitters of series regulators located on heat sink assembly? (see figure 6-6 and 6-9 for voltage levels and power transistor location.)

NO

Failure of series regulator or power supply, supplying the effected output voltage, (refer to figure 6-6 Power Supply Schematic.)

YES

Is the proper 1 MHz signal present at the INPUT/MON rear panel connector J5 when the mode switch is in test and the INT/EXT switch is in the INT position? Verify that the waveform swings from a minimum of 0 to +0.2 volts to a maximum in excess of +1.4 volts with a duty cycle of approximately 25%.

Table 4-5: Model 784 Sectionalization and Localization (continued)

NO

Failure or malfunction of 1 MHz internal oscillator or switch S8 located on rear panel (refer to figure 6-3 schematic diagram).

YES

Is start marker present on rear panel connector J3 when a signal is applied to INPUT A connector J1.

NO

Failure of input A (Start) circuit (refer to figure 6-1 Input circuit schematic).

YES

Is stop marker present on rear panel connector J4 when a signal is applied to INPUT B connector J2.

NO

Failure of input B (Stop) circuit (refer to figure 6-1 Input circuit schematic).

YES

When the mode switch is placed in any of X1000 (expanded) positions, the last two digits of the display are blanked and the decimal is relocated to decade display "6".

NO

Failure of switch section S7C, blanking control neon lamps' DS1 or DS2 or drive transistors Q19 or Q20.

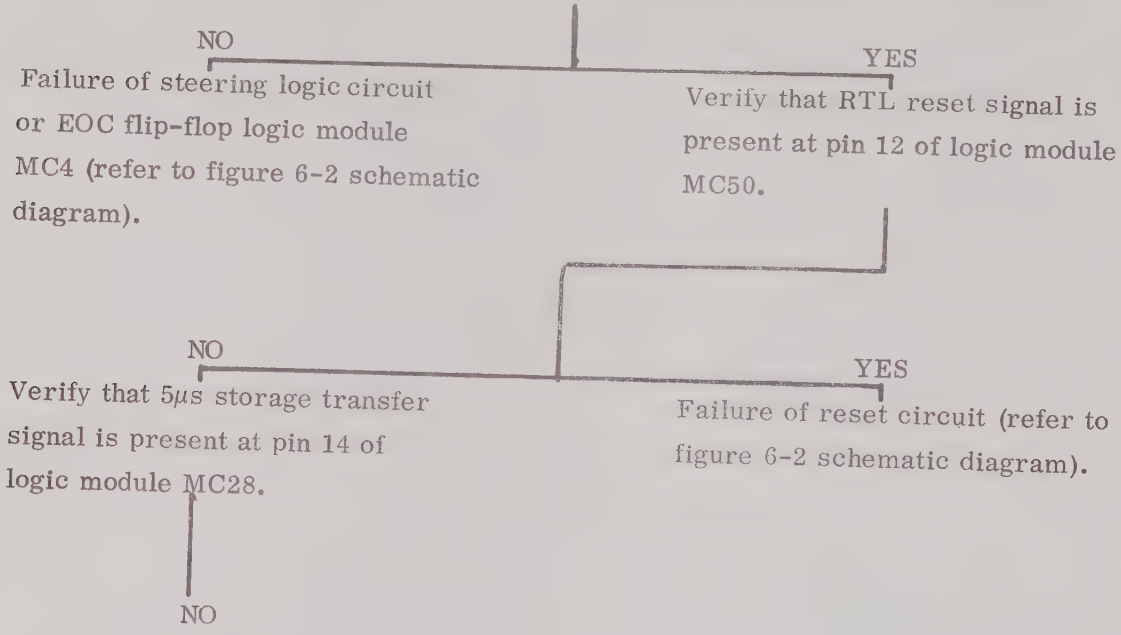
YES

When mode switch is placed in the X1000 (expanded) positions, the signal at pin 1 of logic module MC15 will switch from a high to a low at a ratio of 1000 : 1 to the input signal rate measured at pin 2 of logic module MC10.

NO

Verify that end of count (EOC) signal is present on pin 2 and 9 of of logic module MC28.

Table 4-5: Model 784 Sectionalization and Localization (continued)


NO
YES
Failure of steering logic circuit or EOC flip-flop logic module MC4 (refer to figure 6-2 schematic diagram).
Verify that RTL reset signal is present at pin 12 of logic module MC50.
NO
YES
Verify that 5μs storage transfer signal is present at pin 14 of logic module MC28.
Failure of reset circuit (refer to figure 6-2 schematic diagram).
NO
Failure of storage transfer one-shot logic module MC28, C30, or R114.

4.5.2 Localizations of a malfunction can be accomplished by checking various signals and levels throughout the defective major logic function. A thorough comprehension of the theory of operation (Section 3) combined with the individual schematics (Section 6) should provide sufficient information to confine the malfunction to individual circuit or a logic sub-function.

4.5.3 Isolation

Isolation of the malfunction can normally be accomplished with routine voltage and resistance measurements. Integrated circuit equivalents are included within this section to facilitate their testing, and relationship to their interfacing logic circuits. Whenever a component or P.C. board is replaced, instrument internal adjustments should be checked as necessary (refer to section 4-4).

4.6 REPAIR AND COMPONENT REPLACEMENT TECHNIQUES

Repair and replacement of components should be undertaken only by qualified personnel adept in "solid state" maintenance techniques. When a component failure is encountered, observe these general instructions.

1. Never remove or replace a component or P. C. board while instrument power is enabled.
2. Use only a grounded, transformer-coupled thermostatically controlled soldering iron.
3. Utilize a heat-sink whenever possibility of thermal damage can occur to components or P. C. board pads and tracings.
4. Avoid any application of acid-core type solder.

4.6.1 Power Transistor Replacement.

In the event of a power transistor failure located on the heat-sink transistor assembly, proceed as follows:

1. Remove leads from the display P. C. board.
2. Remove 4-40 screw securing transistor to heat-sink transistor assembly.
3. Coat both sides of the replacement mica washer with thermal conductive grease (Dow Corning compound or 107 or equivalent.)
4. Assemble transistor with mica washer to the heat-sink replacing all hardware.
5. Solder transistor leads into display P. C. board.

4.6.2 Integrated Circuit Replacement

The following instructions outline the proper method for removal and replacement of a defective integrated circuit module.

1. Verify that the integrated circuit in question is, in actuality, defective (refer to the integrated circuit equivalent diagrams contained in section 4.8).

2. On the component side of the P. C. board, carefully clip leads of the defective integrated circuit at the point where the leads enter the plastic case.

3. Remove each individual lead from the component side of the P. C. board with the aid of a soldering iron and long nose pliers.

4. Remove excess solder from P. C. board pads with a pneumatic solder extractor tool.

5. Install the replacement integrated circuit noting correct orientation as depicted by the component location illustration.

6. Solder each lead on the circuit side and all top traces on the component side of the P. C. board.

4.7 REPLACEMENT OF SELECTED COMPONENTS.

A number of instrument components are selected at test for value by circuit effect, when certain components are replaced, selected or not, selection may be required for proper instrument operation. The following paragraphs describe the procedures for component selection as related to operational functions.

4.7.1 Selection of Power Supply Zener Diode References.

The instrument employs five DC voltages which can be adjusted by replacement of selected zener diodes. The +12 volt and -12 volt supplies provide current for the zener diodes of +3.6V, +4.9V and -4.9V supplies and should be selected first. The dc supply voltages and zener diodes are listed below:

+12V ±5%	CR210
-12V ±5%	CR212
+3.6V ±5%	CR205
+4.9V ±5%	CR206
-4.9V ±5%	CR207

4.7.2 Selection of Input Centering Diodes.

The position of the level controls can be adjusted so that the 0 volt level corresponds to the input discriminators triggering at 0 volts, by proper selection of diodes CR4, 5, 6 and 7. Test configuration required for selection is the same as trigger symmetry

adjustments (see figure 4-2 and procedure outlined in table 4-4). The voltage present on display P. C. board pads 17 and 18 is the result of two diode junctions, one being silicon and the other germanium, and should be +1.2 volts and -1.2 volts when diode selection is correct.

4.7.3 Selection of Input Coax Lines (Channel Balance).

The delay between the input A BNC connector J1 and the onset of the A discriminator output at TP1 should equal that of the B channel. If the RG-188/U coax cables connected between the input BNC connectors and the attenuator switches are replaced, they should be cut to length so the channel delay difference is less than ≤1ns. The delays can be monitored at TP1 and 2 located on the logic display PC board in reference to the input BNC connectors J1 and 2. A high speed oscilloscope such as a TEK 475 with sweep set at 10 ns/cm should be used to check delays.

4.7.4 RTL Reset Pulse Width Selection.

The RTL reset pulse width should be 35μs ±10% as monitored at the emitter of transistor Q31. If the reset pulse width is out of tolerance select value of R121 within 1.2K to 3.3K ohm range, 2.2K being nominal the value.

4.7.5 Storage Transfer Pulse Width Selection.

The storage transfer pulse width should be 2 to 8μs, 5μs nominal as monitored at collector of transistor Q25. If the storage transfer pulse width is out of tolerance, select value of R119 for correct width.

4.7.6 First DCU Input J.K. Flip-Flop Selection.

The input flip-flop MC5 is a specially selected JK flip-flop having a part number of SC7355 and can be ordered from Eldorado Electrodata Corp. under manufacturers number EE 5962-004766.

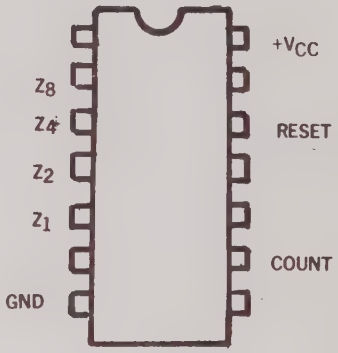
4.8 INTEGRATED CIRCUIT EQUIVALENTS

Circuit equivalents for each type of integrated circuit are described in alpha-numeric sequence within this section. If further information is required, refer to the manufacturer's description.

TABLE OF OUTPUT STATES

COUNT (H=High, L=Low)

	0	1	2	3	4	5	6	7	8	9
Z_1	H	L	H	L	H	L	H	L	H	L
Z_2	H	H	L	L	H	H	L	L	H	H
Z_4	H	H	H	H	L	L	L	L	H	H
Z_8	H	H	H	H	H	H	H	H	L	L



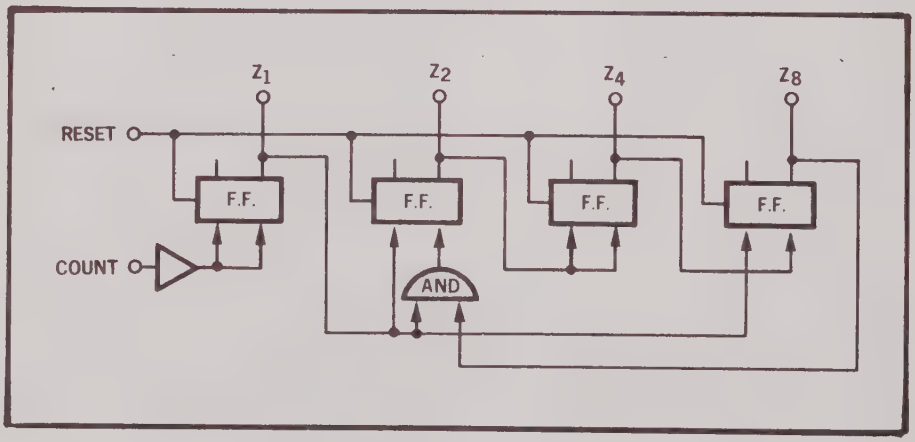
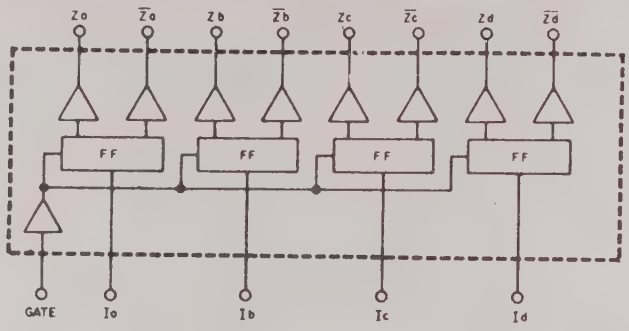
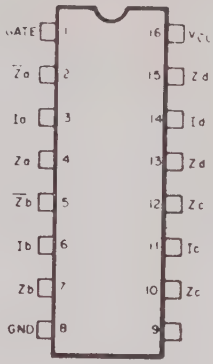


FIGURE 4-3

CμL958 EQUIVALENT



BLOCK DIAGRAM



BASE CONNECTIONS

GATE	I	Z	$\overline{Z}$
L	L	L	H
L	H	H	L
H	ANY	Q	$\overline{Q}$

H = HIGH
L = LOW
Q = THE STATE ASSUMED PRIOR TO "GATE HIGH" IS MAINTAINED

TRUTH TABLE

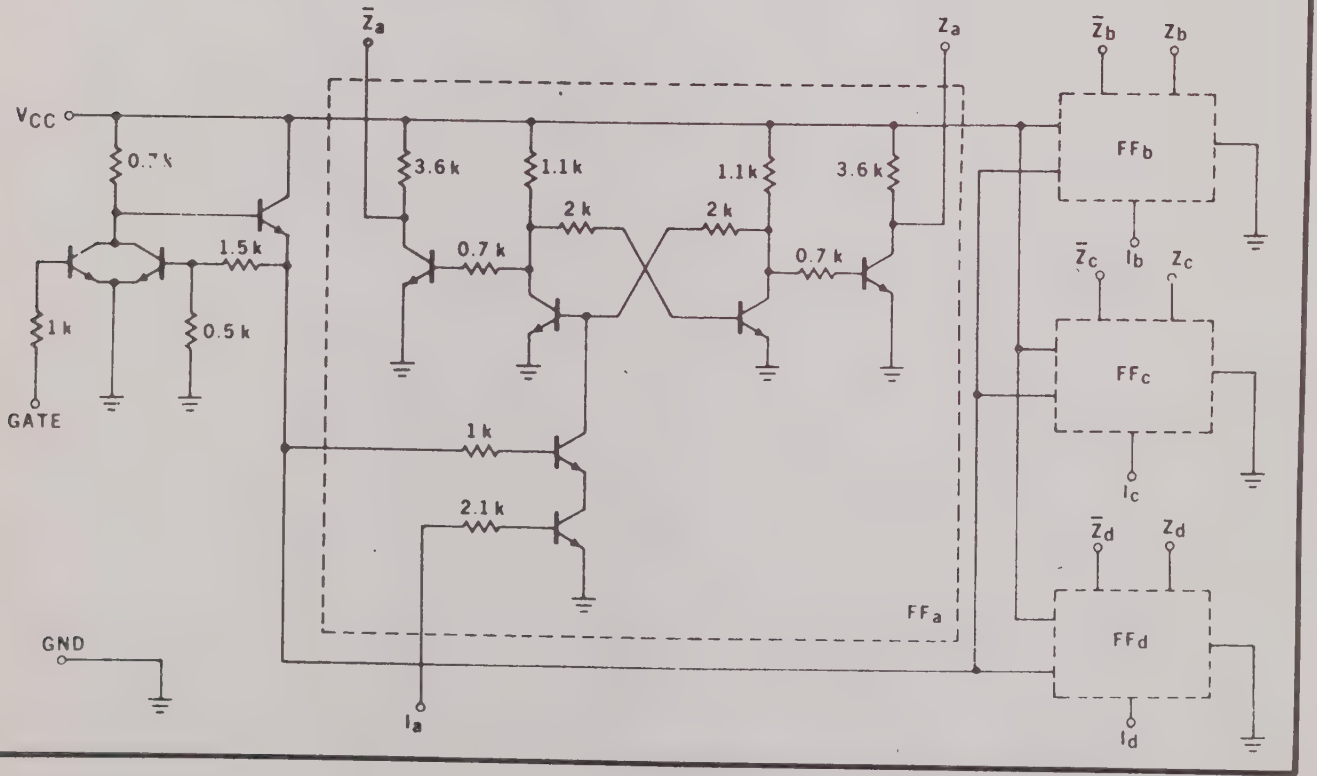


FIGURE 4-4
CμL959 EQUIVALENT

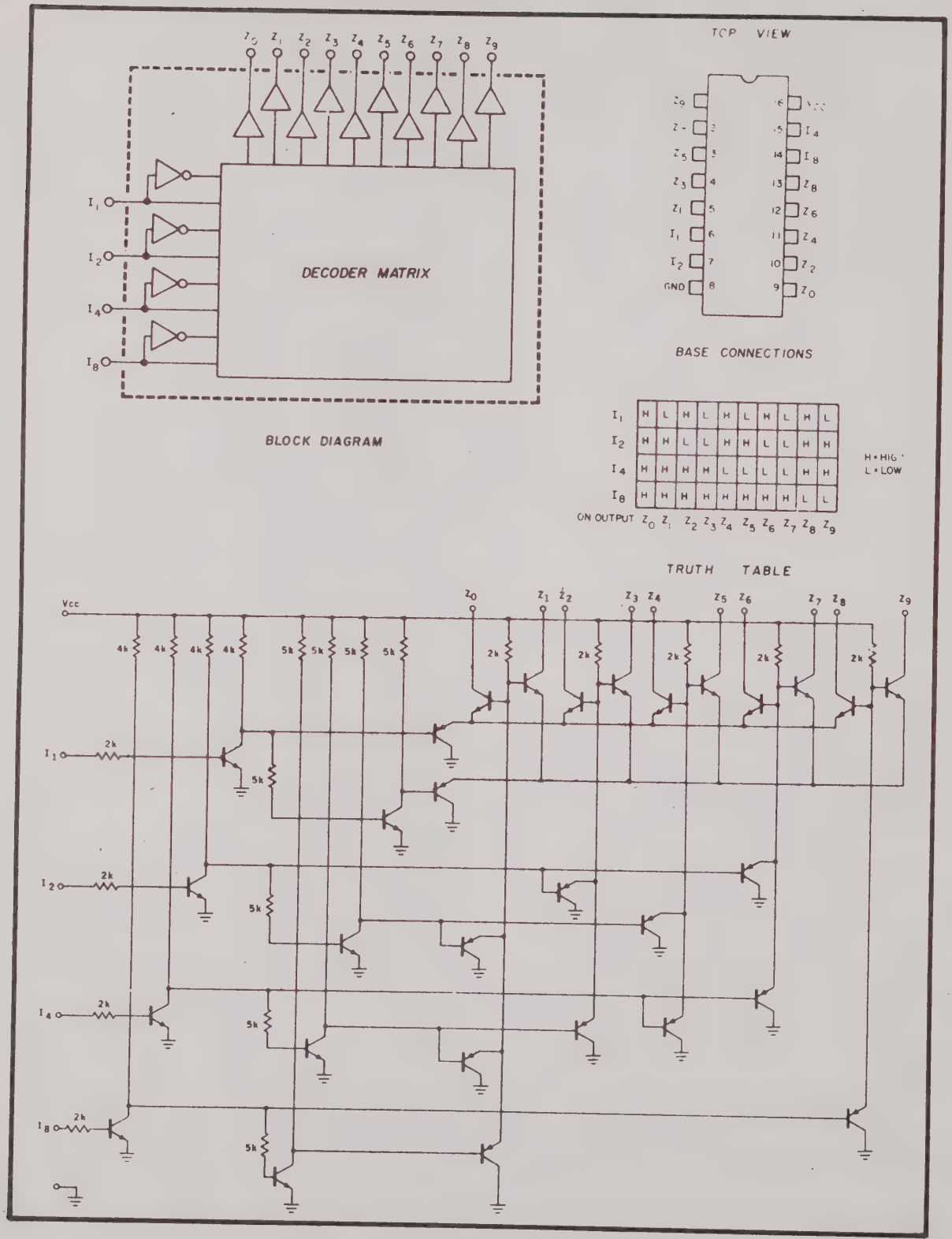
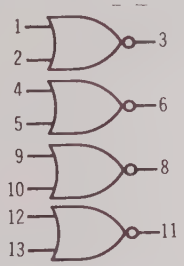


FIGURE 4-5

CμL960 EQUIVALENT

This gate element consists of four 2-input positive logic NOR gate circuits in a single package. The gate circuits may be used independently, or connected together to form flip-flops or non-inverting gates.



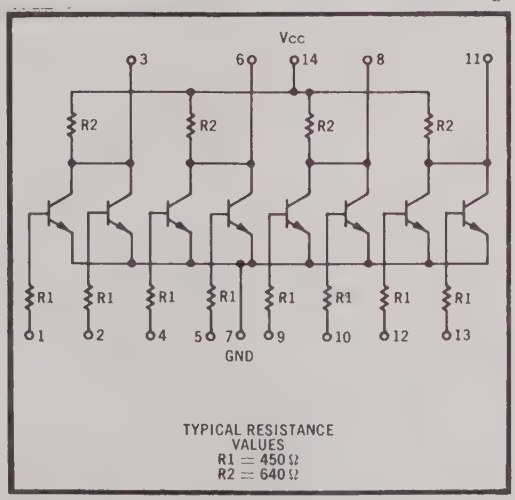
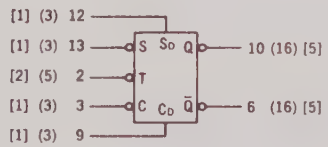


FIGURE 4-6

MC824P EQUIVALENT

J-K flip-flop with direct clear and direct set inputs in addition to the clocked inputs.



1. Direct inputs (C_O and S_O) must be low.
2. The time period prior to the negative transition of the clock pulse is denoted t_n and the time period subsequent to this transition is denoted t_{n+1}.
3. Q_n is the state of the Q output in the time period t_n.
4. Clock (T) to remain unchanged.
5. The output state will not change when the input state goes from $S_O = \bar{C}_D$ to $S_O = C_D = 0$. The output state cannot be predetermined in the case where the input goes from $S_D = C_D = 1$ to $S_O = C_D = 0$.
6. Clock pulse fall time must be < 100 ns.

NUMBER IN PARENTHESIS INDICATES LOADING FACTOR FOR mW MRTL.
NUMBER IN BRACKETS INDICATES LOADING FACTOR FOR MRTL.

$f_{TOG} = 4$ MHz

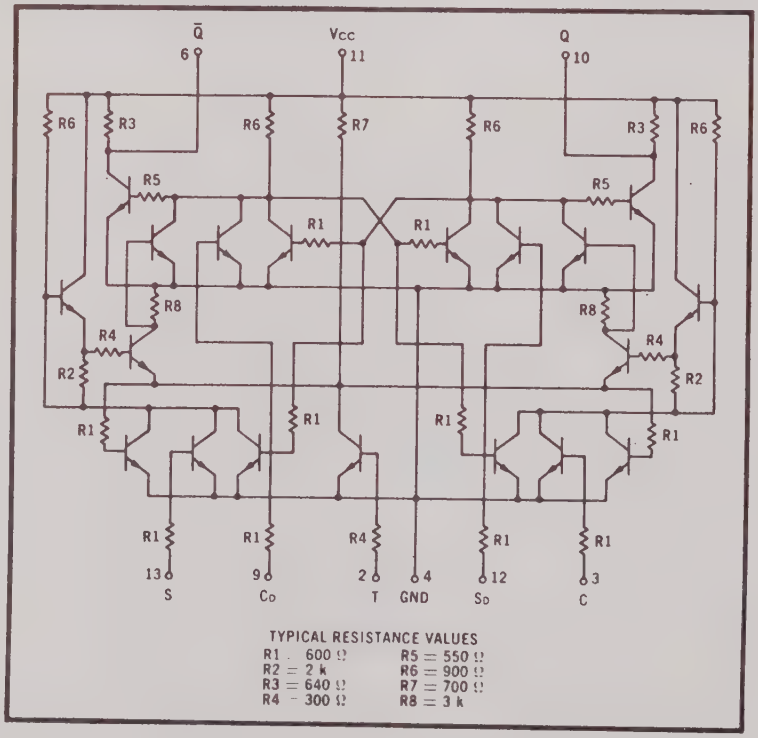
$P_D = 100$ mW (Only Clock Input High)
86 mW (Inputs Low)

CLOCKED INPUT OPERATION ①

t_n ②		t_{n+1} ②	
S	C	Q	$\bar{Q}$
1	1	Q_n ④	$\bar{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\bar{Q}_n$	Q_n ③

DIRECT INPUT OPERATION ①

S_D	C_D	Q	$\bar{Q}$
0	0	③	③
1	0	1	0
0	1	0	1
1	1	0	0

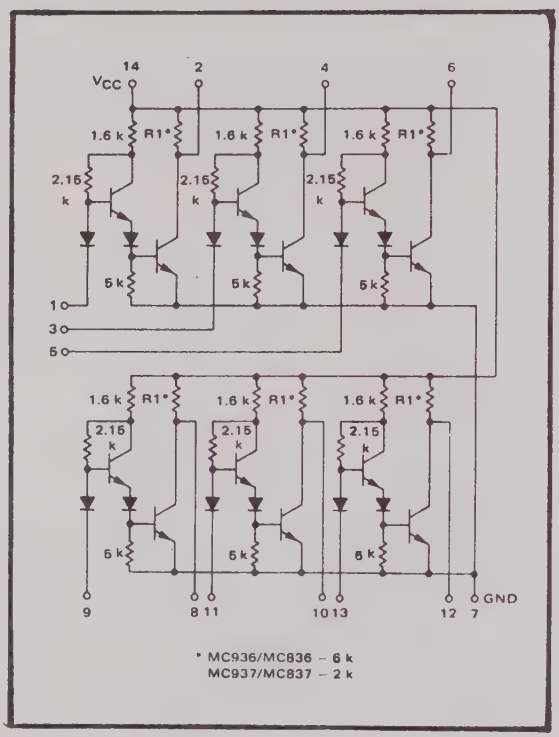


TYPICAL RESISTANCE VALUES

R1 = 600 Ω	R5 = 550 Ω
R2 = 2 k	R6 = 900 Ω
R3 = 640 Ω	R7 = 700 Ω
R4 = 300 Ω	R8 = 3 k

FIGURE 4-7

MC826P EQUIVALENT



This element consists of six inverter circuits.

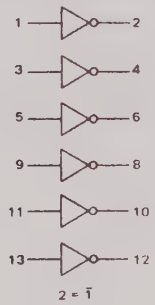
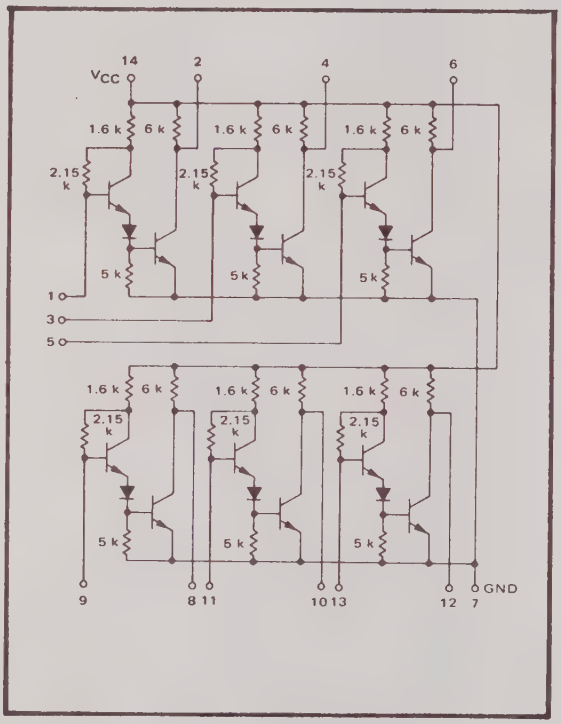
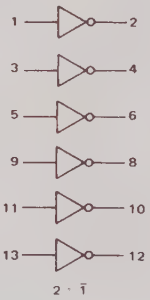


FIGURE 4-8
MC836P EQUIVALENT



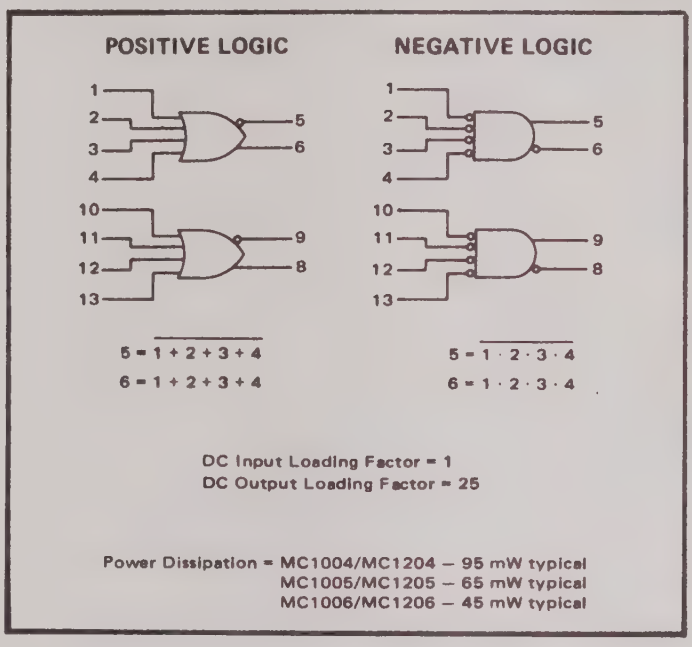
This hex inverter with no input diodes, is useful in applications such as monostable and astable multivibrators. Discrete input diodes may be added to allow translation to MDTL logic from higher voltage levels, or the device may be used in conjunction with gate expanders to form flexible multi-input gate arrays.



Input Loading Factor = 1
Output Loading Factor = 8
Total Power Dissipation = 66 mW typ/pkg
Propagation Delay Time = 30 ns typ

FIGURE 4-9
MC840P EQUIVALENT

Provide simultaneous OR/NOR or AND/NAND output functions. These devices contain an internal bias reference insuring that the threshold point is always in the center of the transition region over the temperature range.



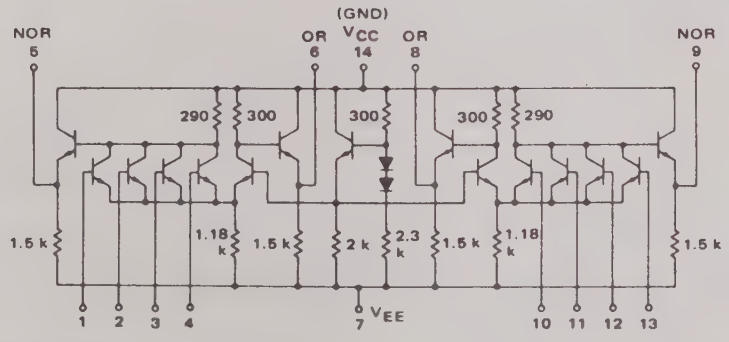
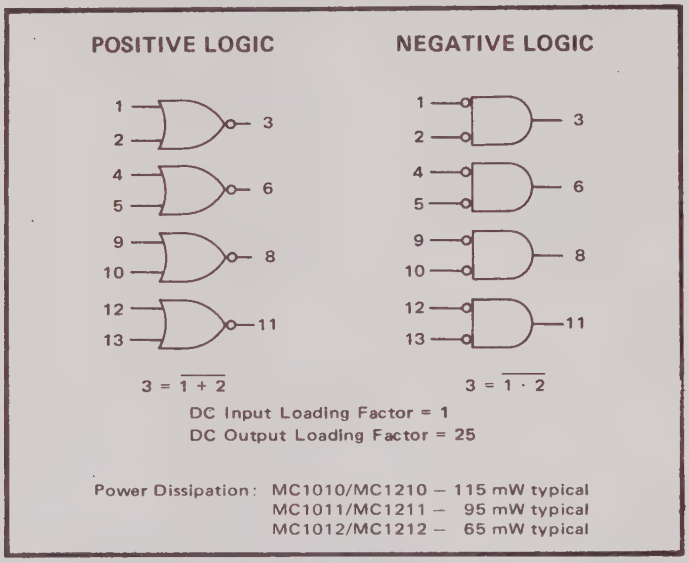


FIGURE 4-10
MC1004P EQUIVALENT

Provide the NOR output function. These devices contain an internal bias reference insuring that the threshold point is always in the center of the transition region over the temperature range.

Emitter follower output configurations differ for these three circuits as shown in the circuit schematic.



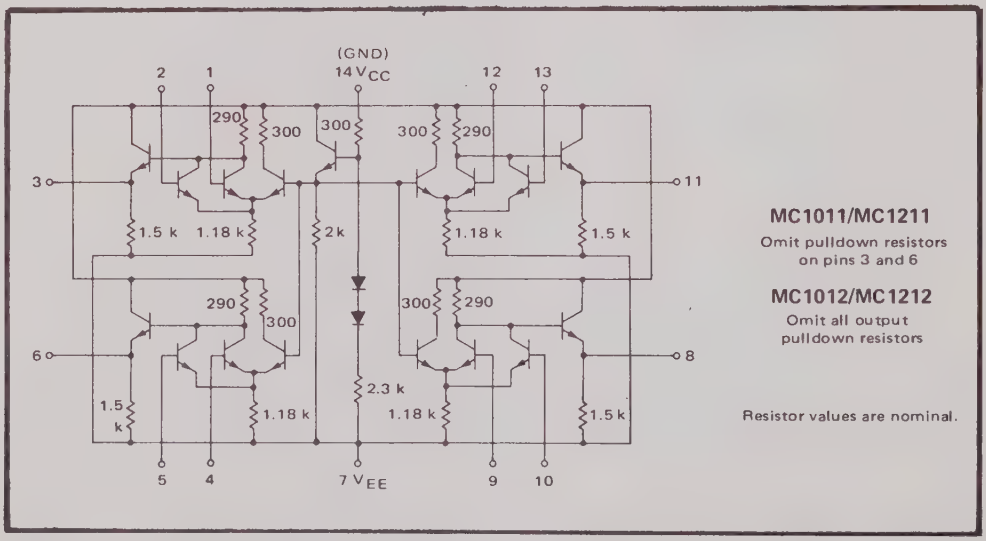
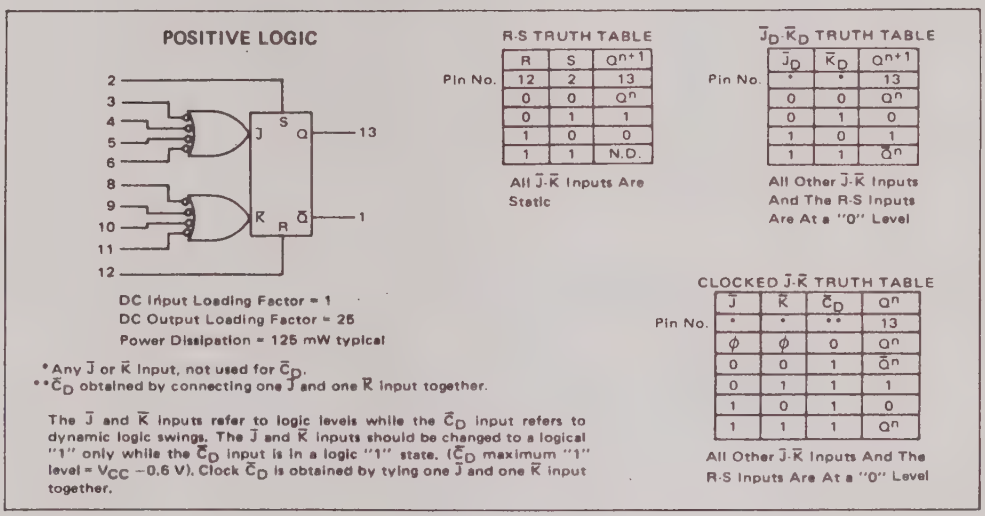


FIGURE 4-11

MC1010P EQUIVALENT


POSITIVE LOGIC
2
3
4
5
6
8
9
10
11
12
J
S
Q
13
K
R
Q̄
1
DC Input Loading Factor = 1
DC Output Loading Factor = 25
Power Dissipation = 125 mW typical
*Any J̄ or K̄ input, not used for C̄D.
**C̄D obtained by connecting one J̄ and one K̄ input together.
The J̄ and K̄ inputs refer to logic levels while the C̄D input refers to dynamic logic swings. The J̄ and K̄ inputs should be changed to a logical "1" only while the C̄D input is in a logic "1" state. (C̄D maximum "1" level = VCC −0.6 V). Clock C̄D is obtained by tying one J̄ and one K̄ input together.
R-S TRUTH TABLE
Pin No.
R S Qn+1
12 2 13
0 0 Qn
0 1 1
1 0 0
1 1 N.D.
All J̄-K̄ Inputs Are Static
J̄D-K̄D TRUTH TABLE
Pin No.
J̄D K̄D Qn+1
* * 13
0 0 Qn
0 1 0
1 0 1
1 1 Q̄n
All Other J̄-K̄ Inputs And The R-S Inputs Are At a "0" Level
CLOCKED J̄-K̄ TRUTH TABLE
Pin No.
J̄ K̄ C̄D Qn
* * ** 13
ϕ ϕ 0 Qn
0 0 1 Q̄n
0 1 1 1
1 0 1 0
1 1 1 Qn
All Other J̄-K̄ Inputs And The R-S Inputs Are At a "0" Level

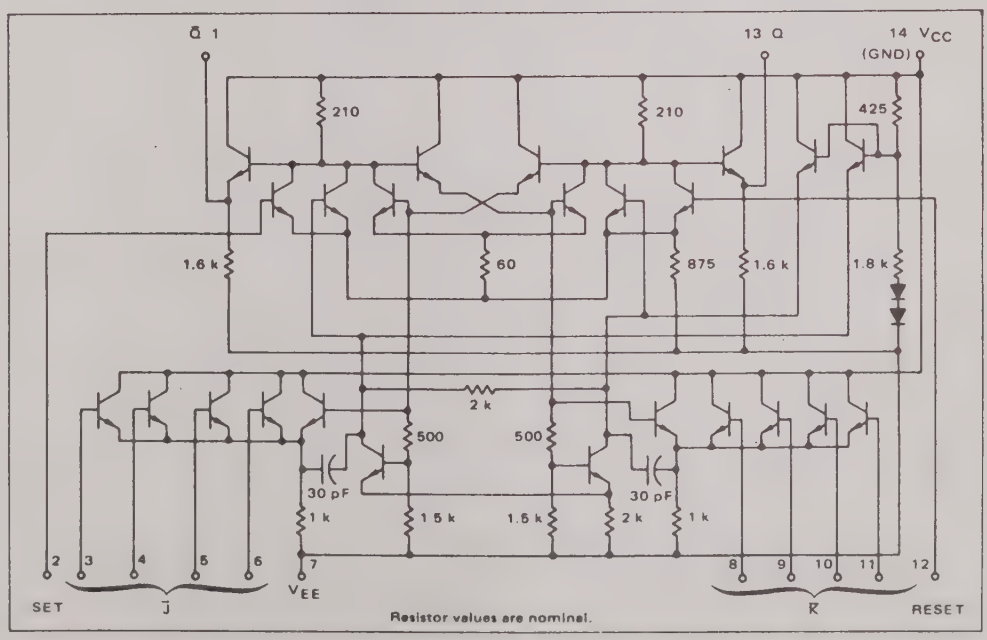
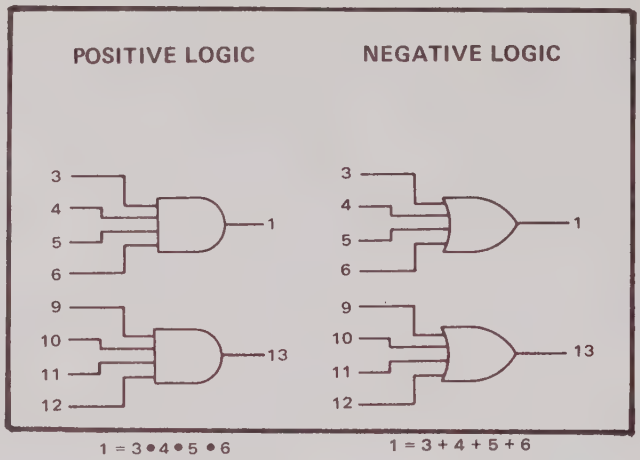


FIGURE 4-12

MC1013P EQUIVALENT



DC Input Loading Factor = 6 (DTL)
DC Output Loading Factor = 25 (MECL)
Power Dissipation = 150 mW typical

Dual level translator intended for converting saturated logic levels to MECL signal levels. The translator provides the positive logic OR function.

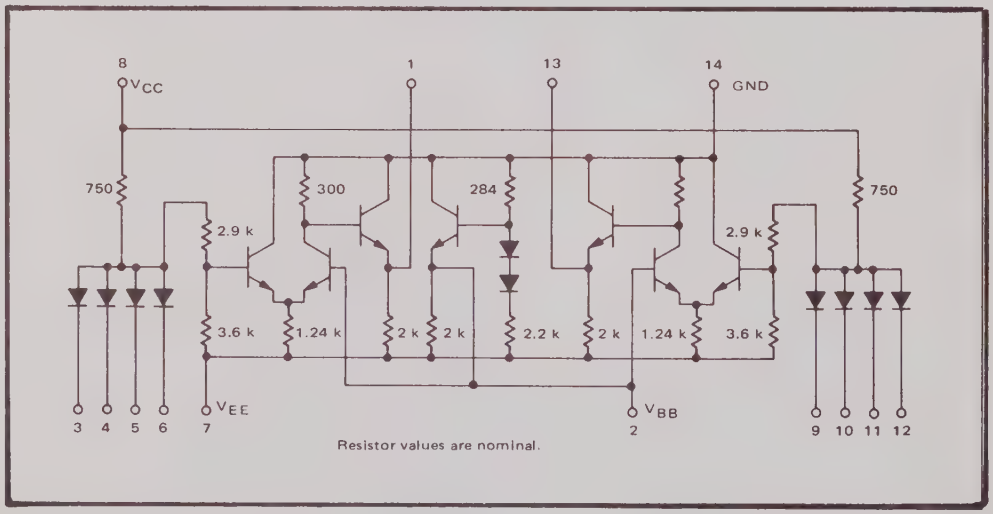
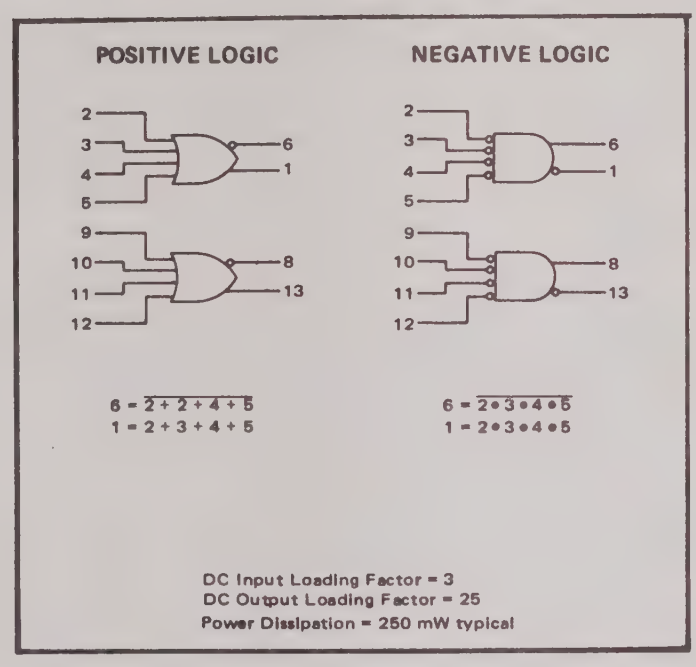


FIGURE 4-13
MC1017P EQUIVALENT

Provides simultaneous OR/NOR or AND/NAND output functions. It contains an internal bias reference insuring that the threshold point is always in the center of the transition region over the temperature range.

This circuit is designed to operate in high-speed digital computer applications as a clock driver or as a high-speed gate.



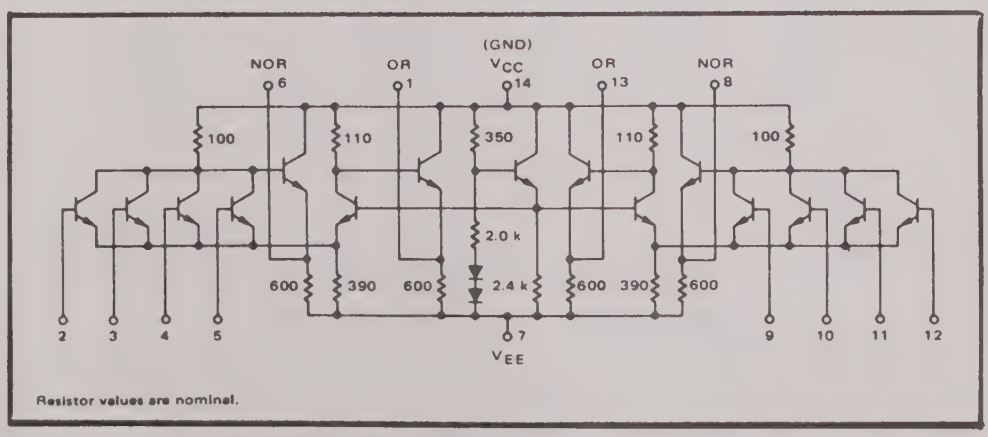
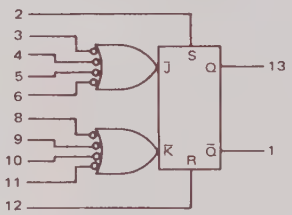


FIGURE 4-14

MC1023P EQUIVALENT

Designed for use at clock frequencies to 100 MHz minimum (120 MHz typical). Logic performing inputs ($\overline{J}$ and $\overline{K}$) are available, as well as dc SET and RESET inputs.

POSITIVE LOGIC



DC Input Loading Factor = 2
DC Output Loading Factor = 25
Power Dissipation = 250 mW typical

R S TRUTH TABLE

Pin No. R	Pin No. S	Q^{n+1}
12	2	13
0	0	Q^n
0	1	1
1	0	0
1	1	N.D.

All $\overline{J}$-$\overline{K}$ Inputs Are Static

$\overline{J}_D$-$\overline{K}_D$ TRUTH TABLE

Pin No. $\overline{J}_D$	Pin No. $\overline{K}_D$	Q^{n+1}
*	*	13
0	0	Q^n
0	1	0
1	0	1
1	1	$\overline{Q}^n$

All Other $\overline{J}$-$\overline{K}$ Inputs And The R-S Inputs Are At a "0" Level

CLOCKED $\overline{J}$-$\overline{K}$ TRUTH TABLE

Pin No. $\overline{J}$	Pin No. $\overline{K}$	$\overline{C}_D$	Q^n
*	*	**	13
ϕ	ϕ	0	Q^n
0	0	1	$\overline{Q}^n$
0	1	1	1
1	0	1	0
1	1	1	Q^n

All Other $\overline{J}$-$\overline{K}$ Inputs And The R-S Inputs Are At a "0" Level

*Any $\overline{J}$ or $\overline{K}$ input, not used for $\overline{C}_D$.
**$\overline{C}_D$ obtained by connecting one $\overline{J}$ and one $\overline{K}$ input together.

The $\overline{J}$ and $\overline{K}$ inputs refer to logic levels while the $\overline{C}_D$ input refers to dynamic logic swings. The $\overline{J}$ and $\overline{K}$ inputs should be changed to a logical "1" only while the $\overline{C}_D$ input is in a logic "1" state. ($\overline{C}_D$ maximum "1" level = V_{CC} −0.6 V). Clock $\overline{C}_D$ is obtained by tying one $\overline{J}$ and one $\overline{K}$ input together.

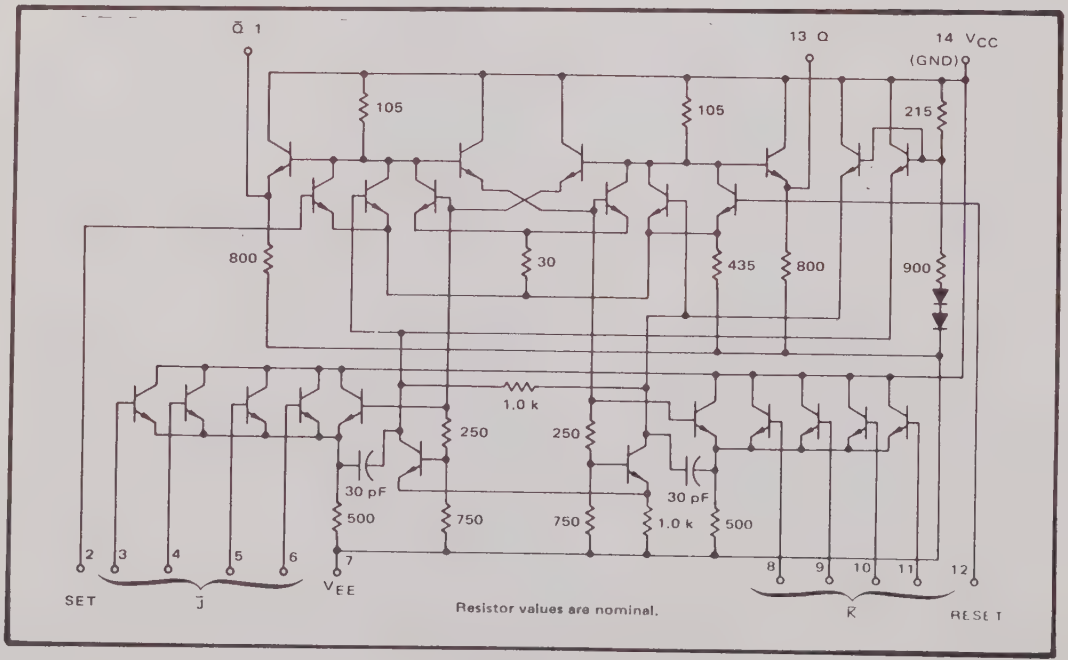
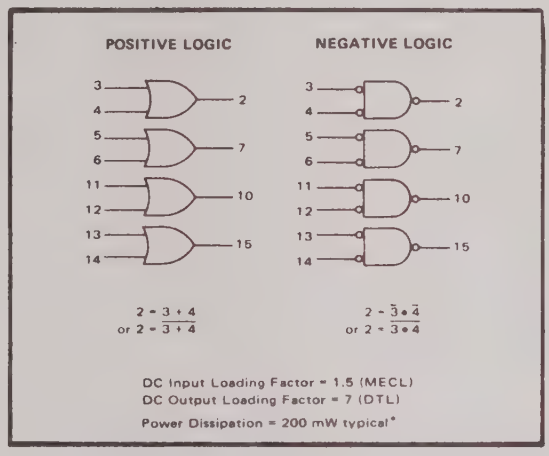


FIGURE 4-15
MC1027P EQUIVALENT

Level translator for converting MECL signal levels to saturated logic levels. The four independent translators provide the positive logic OR function. MC1039 is available in a 16-pin ceramic dual in-line package, Case 620 (add suffix "L" to basic type number).



DC Input Loading Factor = 1.5 (MECL)
DC Output Loading Factor = 7 (DTL)
Power Dissipation = 200 mW typical*

*Sinking 12 mAdc into each output.

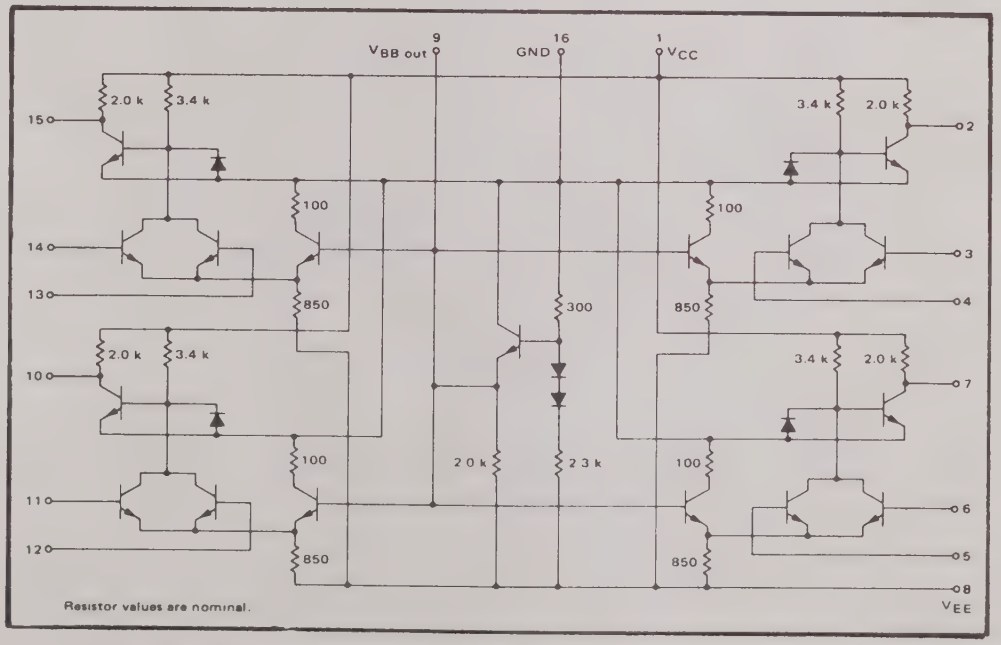
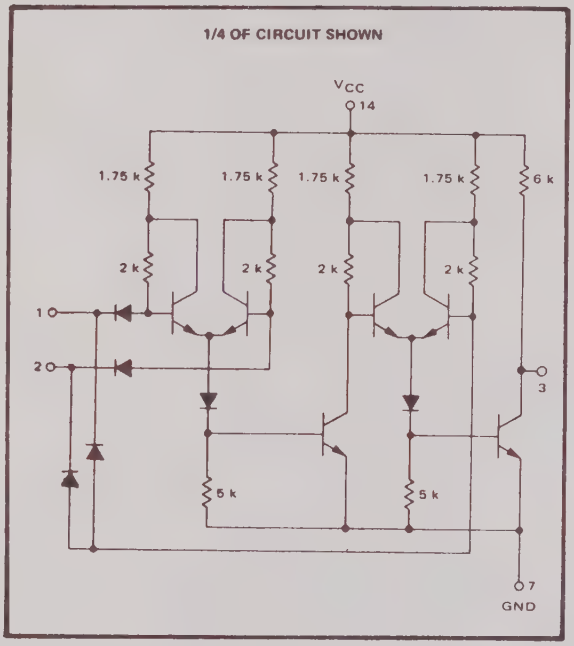
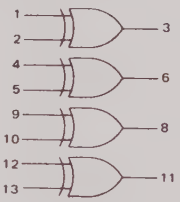


FIGURE 4-16

MC1039P EQUIVALENT

This device consists of four 2-input gates, each performing the logical EXCLUSIVE OR function. Added logic flexibility provided by this device helps to optimize system designs.





Positive Logic: $3 = 1 \bullet \overline{2} + \overline{1} \bullet 2$

Input Loading Factor = 2

Output Loading Factor = 8

Total Power Dissipation:

	MC1912/MC1812
Both Inputs High	115 mW
Both Inputs Low	130 mW
One Low One High	95 mW

Propagation Delay Time = 40 ns typ

LOGIC DIAGRAM
1/4 OF DEVICE SHOWN

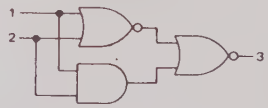


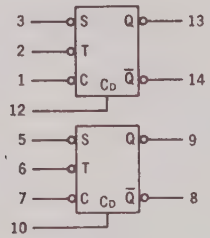
FIGURE 4-17
MC1812P EQUIVALENT

Two J-K flip-flops in a single package. Each flip-flop has a direct clear input in addition to the clocked inputs.

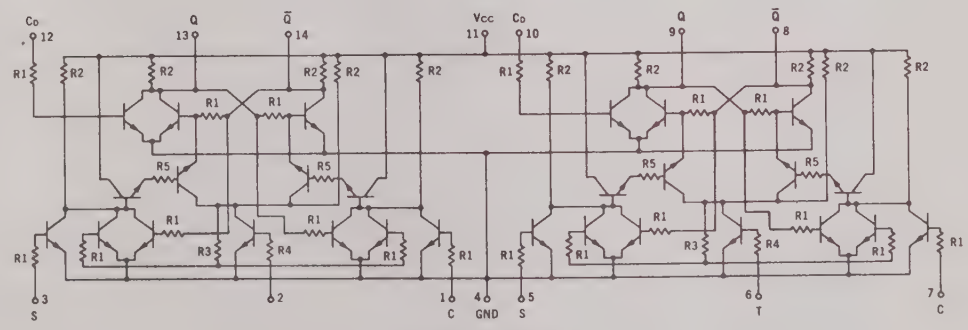
CLOCKED INPUT OPERATION ①

t_n ②		t_{n+1} ②	
S	C	Q	$\bar{Q}$
1	1	Q_n ③	$\bar{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\bar{Q}_n$	Q_n ③

1. Direct input (C_D) must be low.
2. The time period prior to the negative transition of the clock pulse is denoted t_n and the time period subsequent to this transition is denoted t_{n+1}.
3. Q_n is the state of the Q output in the time period t_n.
4. Clock pulse fall time must be < 100 ns.

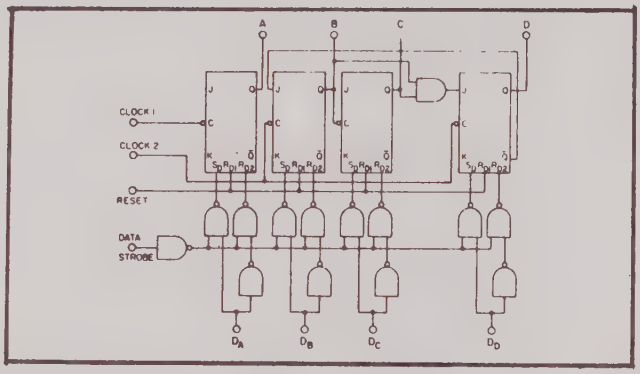


f_{TOG} = 4 MHz
P_D = 182 mW (Only Clock Input High)
158 (Inputs Low)



TYPICAL RESISTANCE VALUES
R1 = 450 Ω R3 = 510 Ω
R2 = 640 Ω R4 = 225 Ω
R5 = 300 Ω

FIGURE 4-18
MC9802P EQUIVALENT



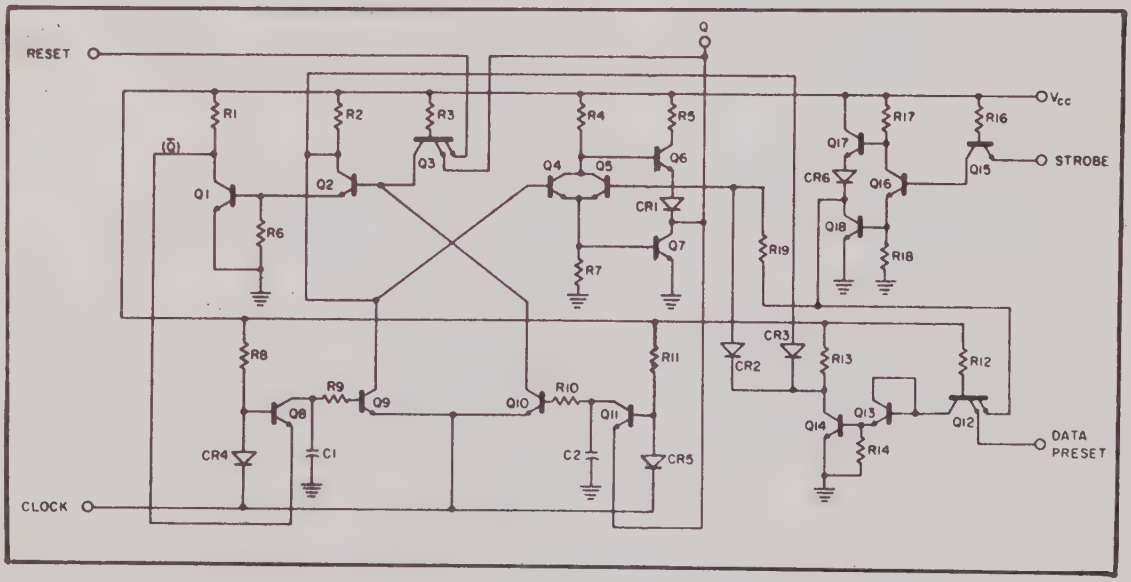
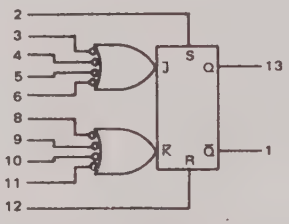


FIGURE 4-19

N8280A EQUIVALENT

Selected component J-K flip-flop for use at clock frequencies above 100 MHz. Provided with logic performing gate inputs (J and K) and dc SET and RESET inputs.

POSITIVE LOGIC



DC Input Loading Factor = 1
DC Output Loading Factor = 25
Power Dissipation = 125 mW typical

*Any J̄ or K̄ input, not used for C̄D.
**C̄D obtained by connecting one J̄ and one K̄ input together.

The J̄ and K̄ inputs refer to logic levels while the C̄D input refers to dynamic logic swings. The J̄ and K̄ inputs should be changed to a logical "1" only while the C̄D input is in a logic "1" state. (C̄D maximum "1" level = V_{CC} −0.6 V). Clock C̄D is obtained by tying one J̄ and one K̄ input together.

R-S TRUTH TABLE

Pin No.	R 12	S 2	Q^{n+1} 13
	0	0	Q^n
	0	1	1
	1	0	0
	1	1	N.D.

All J̄-K̄ Inputs Are Static

J̄D-K̄D TRUTH TABLE

Pin No.	J̄D *	K̄D *	Q^{n+1} 13
	0	0	Q^n
	0	1	0
	1	0	1
	1	1	$\bar{Q}^n$

All Other J̄-K̄ Inputs And The R-S Inputs Are At a "0" Level

CLOCKED J̄-K̄ TRUTH TABLE

Pin No.	J̄ *	K̄ *	C̄D **	Q^n 13
	ϕ	ϕ	0	Q^n
	0	0	1	$\bar{Q}^n$
	0	1	1	1
	1	0	1	0
	1	1	1	Q^n

All Other J̄-K̄ Inputs And The R-S Inputs Are At a "0" Level

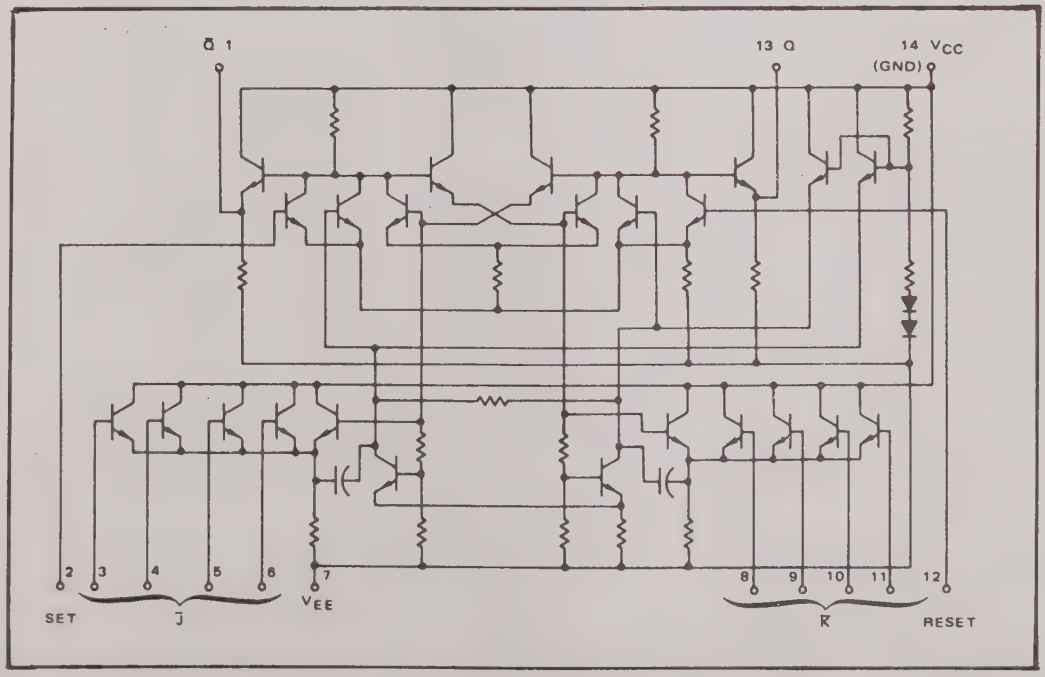


FIGURE 4-20
SC7355P EQUIVALENT

SECTION 5
PARTS LIST

SECTION 5

PARTS LIST

5.1 INTRODUCTION

This section contains the necessary information for the procurement of replacement parts from either Eldorado Electrodata or directly from commercial sources.

The parts lists are divided into separate sub-assemblies with the individual components arranged in alpha-numeric succession. To obtain information pertaining to a component first refer to the parts list for the particular assembly then index the component in question with the left hand "reference" column.

5.2 ORDERING INFORMATION

When it is necessary to order replacement parts directly from Eldorado Electrodata address all orders or inquires to:

ELDORADO INSTRUMENTS CO
2495 Estand Way
Pleasant Hill, CA 94523
(415) 682-2100

When ordering replacement parts be certain to specify instrument model and serial number and complete part description including reference, description, manufacturer, manufacturer's part number and the six digit Eldorado part number.

5.3 CODE OF MANUFACTURERS

Component manufacturers have been abbreviated in the parts lists with either a two, three or four character code. The following table cross-references the abbreviation with the full name and address of the selected commercial source.

TABLE 5-1

CODE OF MANUFACTURERS

AB	Allen Bradley Co., Milwaukee, Wisconsin
AML	Amphenol Electronic Corp., Chicago, Illinois
AMPE	Amperex Electronics Corp., Hauppauge, New York
AUTO	Automatic Metal Products Corp., Brooklyn, New York
BECK	Beckman Instruments, Helipot Dov., Fullerton, California
BURR	Burroughs Corp., Plainfield, New Jersey
CDC	Continental Device Corp., Hawthorne, California
CONW	Continental-Wirt Electronics Corp., Philadelphia, Pennsylvania
CRL	Centralab, Milwaukee, Wisconsin
DEL	Delevan Electronics Corp., Aurora, New York
DIAL	Dialight Corp., Brooklyn, New York
EE	Eldorado Electrodata Corp., Concord, California
ERIE	Erie Technological Products, Erie Pennsylvania
FAI	Fairchild Semiconductor, Mountain View, California
FILT	Filtaire, Inc., Charlottesville, Virginia
GE	General Electric Co., Auburn, New York
GRAY	Grayhill, Inc., LaGrange, Illinois
HPA	Hewlett Packard Associates, Palo Alto, California
ITT	ITT Semiconductors, West Palm Beach, Florida
JONS	E.F. Johnson Co., Waseca, Minnesota
LTTL	Littelfuse, Inc., DesPlaines, Illinois
MAL	Mallory Capacitor Co., Indianapolis, Indiana
MOT	Motorola, Phoenix, Arizona
PAM	Pamotor, Inc., Burlingame, California
PIC	Pacific Instrument Co., Oakland, California
POTT	Potter-Englewood Corp., Inglewood, California
RAY	Raytheon Semiconductors, Mountain View, California
REC	Republic Electronics Corp., Paterson, New Jersey
SAN	Sangamo Electric Co., Springfield, Illinois
SEA	Sealectro, Mamaroneck, New York
SIG	Signetics Corp., Sunnyvale, California
SOL	Solitron Devices, Piviera Beach, Florida
SPR	Sprague Electric, North Adams, Massachusetts
STM	STM Corporation, Oakland, California
SWT	Switchcraft, Inc., Chicago, Illinois
SYL	Sylvania Electric Products, Inc., Woburn, Massachusetts
TI	Texas Instruments, Dallas, Texas
VIT	Vitramon, Inc., Bridgeport, Connecticut
VOL	Voltronics Corp., Hanover, New Jersey

PARTS LIST
DISPLAY BOARD

Reference	Description	Mfr.	Mfr. No.	EE No.	Qty.
	Display Board PC Assembly	EE	C-33-06413	046413	1
	Display PC Board	EE	C-79-05927	045927	1
C1, 2, 4, 6, 7, 9, 11, 22, 24, 40, 41	Capacitor, Mylar .1 μF, 250 wvdc	AMPE	C280AE/P100K	000211	11
C3, 8	Capacitor, Ceramic Disc. .001 μF, 1000 wvdc	CRL	DD-102	000116	2
C5, 10, 12, 25, 26, 27, 28, 29, 31, 32, 42, 43	Capacitor, Ceramic Disc. .01 μF, 100 wvdc	SPR	TG-S10	000158	12
C13, 35	Capacitor, Ceramic Disc. 5000 pF, 100 wvdc	SPR	TG-D50	000150	2
C14	Capacitor, Dipped Mica 270 pF, 500 wvdc	SAN	D155F271JO	000091	1
C15	Capacitor, Dipped Mica Factory Select (33 pF nom.)	SAN	D155F Series	000059	1
C16	Capacitor, Ceramic Disc. 150 pF, 1000 wvdc	CRL	DD-151	000085	1
C17	Capacitor, Variable 1.5-11.6 pF	JONS	189-50A-5	003037	1
C18	Capacitor, Dipped Mica Factory Select (5 pF nom.)	JFD		000028	1
C19	Capacitor, Ceramic 22 pF, 50 wvdc	MUCON	1U22RK	003007	1
C20	Capacitor, Dipped Mica 560 pF, 500 wvdc	SAN	D155F561JO	000104	1
C21	Capacitor, Ceramic Disc. 470 pF, 100 wvdc	CRL	DD-471	000103	1
C23	Capacitor, Dipped Mica 33 pF, 500 wvdc	SAN	D155F330JO	000059	1
C30	Capacitor, Ceramic Disc. .0022 μF, 100 wvdc	VIT	DD-222	000130	1
C33	Capacitor, Ceramic .022 μF, 100 wvdc	GUL	CK06BX223K	000179	1
C34	Capacitor, Electrolytic 4.7 μF, 35 wvdc	MAL	CS13BF475K	003025	1
C36, 39	Capacitor, Dipped Mica 1000 pF, 25 wvdc	STM		003032	2

Reference	Description	Mfr.	Mfr. No.	EE No.	Qty.
C37, 38	Capacitor, Dipped Mica 47 pF, 500 wvdc	SAN	D155F470JO	000065	2
CR1, 2, 6, 7	Diode, 1N459A	TI	1N459A	000520	4
CR3, 4, 8, 9	Diode, HPA2900	HPA	HPA2900	003425	4
CR5, 10	Diode, Tunnel TD253A	GE	TD253A	000509	2
CR11, 14, 16, 17	Diode, 1N3605	ITT	1N3605	000550	4
CR12, 13	Diode, 1N695	SYL	1N695	000523	2
CR15	Diode, CD2496 (3-1001)	CDC	CD2496	000570	1
D7	Coax Cable RG 196 40" long	EE			1
DS1, 2	Lamp, Neon NE83	GE	NE83	003506	2
L1, 2, 4, 5	Inductor .15 μH, 10%	DEL	1025-00	000647	4
L3, 6	Inductor .33 μH, 10%	DEL	1025-08	000650	2
L7, 8	Inductor 180 μH, 5%	DEL	1537-88	000729	2
MC1, 9, 11, 21	Micromodule, MC1027P 120 MHz J-K Flip-flop	MOT	MC1027P	003112	4
MC2, 10	Micromodule, MC1010P Quad 2-Input NOR Gate	MOT	MC1010P	003502	2
MC3	Micromodule, MC1023P Dual 4-Input Clock Driver	MOT	MC1023P	003111	1
MC4, 6, 7, 8, 22, 23, 24	Micromodule, MC1013P 85 MHz J-K Flip-flop	MOT	MC1013P	003105	7
MC5	Micromodule, SC7355P Selected J-K Flip-flop	EE	SC7355P	004766	1
MC12	Micromodule, MC1004P Dual 4-Input OR/NOR Gate	MOT	MC1004P	003109	1
MC13, 14	Micromodule, MC1039P MECL-to-Saturated Logic Quad Converter	MOT	MC1039P	003503	2
MC15	Micromodule, MC1017P Saturated Logic-to-MECL Translator	MOT	MC1017P	003504	1
MC16, 27, 32	Micromodule, N8280A Presettable Decade Counter	SIG	N8280A	004801	3
MC17, 18, 19, 26	Micromodule, MC9802P Dual J-K Flip-flop	MOT	MC9802P	003564	4
MC20, 25, 28, 29	Micromodule, MC824P Quad 2-Input Gate	MOT	MC824P	000871	4

Note: D1 through D6 are not used.

Reference	Description	Mfr.	Mfr. No.	EE No.	Qty.
MC30, 33, 36, 39, 42, 45, 48, 51	Micromodule, CμL959 Buffer Register	FAI	CμL959	003102	8
MC31, 34, 37, 40, 43, 46, 49, 52	Micromodule, CμL960 Decimal Decoder	FAI	CμL960	003103	8
MC35, 38, 41, 44, 47, 50	Micromodule, CμL958 Decade Counter	FAI	CμL958	003101	6
MC53	Micromodule, MC826P J-K Flip-flop	MOT	MC826P	000872	1
Q1, 2, 6, 8, 9, 10, 13, 16, 29	Transistor, 2N3640	FAI	2N3640	001728	9
Q3, 4, 5, 7, 11 12, 14, 15, 17, 18, 21, 24, 30, 31, 32	Transistor, 2N3646	FAI	2N3646	001731	15
Q19, 20	Transistor, 4-1007	EE	4-1007	001759	2
Q22, 23	Transistor, 2N2924	GE	2N2924	001716	2
Q25	Transistor, 2N4124	MOT	2N4124	003294	1
Q26	Transistor, 2N3569	FAI	2N3569	001824	1
Q27	Transistor, 2N3702	TI	2N3702	001733	1
Q28	Transistor, TIS43	TI	TIS43	001751	1
R6, 33	Resistor, Carbon Comp. 68Ω, 1/4W, 5%	AB	CB6805	001079	2
R7, 34, 118	Resistor, Carbon Comp. 1.8k, 1/4W, 5%	AB	CB1825	001101	3
R8, 13, 18, 35, 40, 45, 123, 130, 131	Resistor, Carbon Comp. 330Ω, 1/4W, 5%	AB	CB3315	001090	9
R9, 36, 109, 129	Resistor, Carbon Comp. 2.2k, 1/4W, 5%	AB	CB2225	001103	4
R10, 12, 22, 25, 37, 39, 49, 52, 92	Resistor, Carbon Comp. 470Ω, 1/4W, 5%	AB	CB4715	001092	9
R11, 16, 29, 38, 43, 56, 94, 115	Resistor, Carbon Comp. 100Ω, 1/4W, 5%	AB	CB1015	001081	8
R14, 15, 41, 42	Resistor, Carbon Comp. 560Ω, 1/4W, 5%	AB	CB5615	001094	4
R19, 21, 46, 48, 75, 76, 77, 78, 102, 111	Resistor, Carbon Comp. 680Ω, 1/4W, 5%	AB	CB6815	001096	10

Reference	Description	Mfr.	Mfr. No.	EE No.	Qty.
R20, 47	Resistor, Carbon Comp. 18Ω, 1/4W, 5%	AB	CB1805	001070	2
R23, 30, 50, 57, 60, 61	Resistor, Carbon Comp. 220Ω, 1/4W, 5%	AB	CB2215	001086	6
R24, 51	Potentiometer, 500Ω	BECK	62PR500	000956	2
R26, 53	Resistor, Carbon Comp. 56Ω, 1/4W, 5%	AB	CB5605	001077	2
R27, 54, 69, 72, 73, 74, 79, 80, 108, 113, 116, 119, 125, 128, 132, 133	Resistor, Carbon Comp. 1k, 1/4W, 5%	AB	CB1025	001098	16
R28, 55, 98	Resistor, Carbon Comp. 1.2k, 1/4W, 5%	AB	CB1225	001099	3
R31, 32, 58, 59, 122	Resistor, Carbon Comp. 180Ω, 1/4W, 5%	AB	CB1815	001084	5
R67, 95	Resistor, Carbon Comp. 2.7k, 1/4W, 5%	AB	CB2725	001105	2
R68, 91, 97, 110, 117, 127	Resistor, Carbon Comp. 3.3k, 1/4W, 5%	AB	CB3325	001107	6
R70, 96, 99	Resistor, Carbon Comp. 47Ω, 1/4W, 5%	AB	CB4705	001075	3
R71	Resistor, Carbon Comp. Factory Select (510Ω nom.)	AB	CB Series	001093	1
R81-88	Resistor, Carbon Comp. 33k, 1/2W, 5%	AB	EB3335	001216	8
R89, 90	Resistor, Carbon Comp. 22k, 1/4W, 5%	AB	CB2235	001120	2
R93	Resistor, Carbon Comp. 47k, 1/4W, 5%	AB	CB4735	001124	1
R100	Resistor, Carbon Comp. 15k, 1/4W, 5%	AB	CB1535	001118	1
R101	Resistor, Carbon Comp. 8.2k, 1/4W, 5%	AB	CB8225	001115	1
R105	Resistor, Carbon Comp. 3.9k, 1/4W, 5%	AB	CB3925	001108	1
R107	Resistor, Carbon Comp. 33Ω, 1/4W, 5%	AB	CB3305	001073	1
R112, 126	Resistor, Carbon Comp. 10k, 1/4W, 5%	AB	CB1035	001116	2
R114	Resistor, Carbon Comp. 2.4k, 1/4W, 5%	AB	CB2425	001104	1

Reference	Description	Mfr.	Mfr. No.	EE No.	Qty.
R120	Resistor, Carbon Comp. 82Ω, 1/4W, 5%	AB	CB8205	001080	1
R121	Resistor, Carbon Comp. Factory Select (2.2k nom.)	AB	CB Series	001103	1
R124	Resistor, Carbon Comp. 5.6k, 1/4W, 5%	AB	CB5625	001111	1
S1, 2	Not Used				
S7	Switch, Rotary	EE	B-93-09185	005019	1
T1, 3	Transformer	EE	B-02-06410	046410	2
T2, 4	Transformer	EE	B-02-08699	048699	2
V1-8	Tube, Numerical Indicator	BURR	B5750	003279	8
Y1	Crystal, 1 MHz (Red Dot)	FILT	CR-18/U	003049	1

PARTS LIST
POWER SUPPLY
(Part of Display Board)

Reference	Description	Mfr.	Mfr. No.	EE No.	Qty.
C201, 202	Capacitor, Electrolytic 8000 μF, 12 wvdc	STM	91C12SH83	003036	2
C203	Capacitor, Electrolytic 2 μF, 350 wvdc	MAL	TC595	003022	1
C204	Capacitor, Electrolytic 250 μF, 25 wvdc	AMPE	C437ARF250	003030	1
C205	Capacitor, Electrolytic 1000 μF, 25 wvdc	STM	23C24TS13	003032	1
C206	Capacitor, Ceramic Disc. .01 μF, 100 wvdc	SPR	TG-S10	000158	1
CR201, 202, 203, 204	Diode, 2A100	SOL	2A100	000568	4
CR205, 213	Diode, Zener, 1N749A	MOT	1N749A	000527	2
CR206, 207	Diode, Zener, 1N752A	MOT	1N752A	000530	2
CR208	Diode, 1N4005	ITT	1N4005	003063	1
CR209	Bridge Rectifier, MDA920A-2	MOT	MDA920A-2	003053	1
CR210, 212	Diode, Zener, 1N759A	MOT	1N759A	000537	2
CR211	Diode, 1N3605	RAY	1N3605	000550	1
Q201, 204, 205, 211	Transistor, 2N3646	FAI	2N3646	001731	4
Q202	Transistor, 2N3053	RAY	2N3053	001719	1
Q207	Transistor, 2N3640	FAI	2N3640	001728	1
Q208	Transistor, 2N4890	MOT	2N4890	003271	1
R201	Resistor, Carbon Comp. 820Ω, 1/4W, 5%	AB	CB8215	001097	1
R202	Resistor, Carbon Comp. 330Ω, 1/2W, 5%	AB	EB3315	001187	1
R203	Resistor, Carbon Comp. 180Ω, 1/4W, 5%	AB	CB1815	001084	1
R204, 212	Resistor, Carbon Comp. 270Ω, 1/4W, 5%	AB	CB2715	001088	2
R205, 209	Resistor, Carbon Comp. 680Ω, 1/4W, 5%	AB	CB6815	001096	2
R206, 210	Resistor, Carbon Comp. 390Ω, 1/2W, 5%	AB	EB2915	001182	2

Reference	Description	Mfr.	Mfr. No.	EE No.	Qty.
R207, 218	Resistor, Carbon Comp. 220Ω, 1/4W, 5%	AB	CB2215	001086	2
R208	Resistor, Carbon Comp. 51Ω, 1/4W, 5%	AB	CB5105	001076	1
R211	Resistor, Carbon Comp. 150Ω, 1/4W, 5%	AB	CB1515	001083	1
R213	Resistor, Carbon Comp. 120Ω, 1/4W, 5%	AB	CB1215	001082	1
R214	Resistor, Carbon Comp. 1MΩ, 1/4W, 5%	AB	CB1055	001145	1
R215	Resistor, Carbon Comp. 270Ω, 1/2W, 5%	AB	EB2715	001179	1
R216	Resistor, Carbon Comp. 6.8Ω, 1W, 5%	AB	GB68G	001257	1
R217	Resistor, Carbon Comp. 3.9k, 1/4W, 5%	AB	CB3925	001108	1
R219	Resistor, Carbon Comp. 10Ω, 1W, 5%	AB	GB1005	001258	1
R220	Resistor, Carbon Comp. 1k, 1/4W, 5%	AB	CB1025	001098	1
T201	Transformer	PIC	T-1394	003250	1

PARTS LIST

100 MHz VCO

Reference	Description	Mfr.	Mfr. No.	EE No.	Qty.
	VCO PC Board Assembly	EE	B-33-05403	046403	1
	VCO PC Board	EE	B-79-06169	046169	1
C1	Capacitor, Ceramic Disc .002 μF, 100 wvdc	ERIE	825-Z5U-202P	000127	1
C2, 3	Capacitor, Dipped Mica 22 pF, 500 wvdc	SAN	D155F220JO	000050	2
C4	Capacitor, Variable .8-10 pF, 250 wvdc	VOL	AF10	003473	1
C5	Capacitor, Dipped Mica 5 pF, 500 wvdc	SAN	D155F050JO	000028	1
C6, 7, 8, 9	Capacitor, Ceramic Disc .01 μF, 100 wvdc	SPR	TG-S10	000158	4
CR1, 2	Diode, MV1620	MOT	MV1620	003056	2
L1, 3	Inductor, .82 μH	DEL	1025-18	000656	2
L2	Inductor, 180 μH			000729	1
Q1, 4	Transistor, 2N3646	FAI	2N3646	001731	2
Q2, 3	Transistor, MPSL08	MOT	MPSL08	003501	2
R1, 11	Resistor, Carbon Comp. 47Ω, 1/4W, 5%	AB	CB4705	001075	2
R2, 10	Resistor, Carbon Comp. 560Ω, 1/4W, 5%	AB	CB5615	001094	2
R3, 4, 9, 12	Resistor, Carbon Comp. 150Ω, 1/4W, 5%	AB	CB1515	001083	4
R5, 6, 7, 8	Resistor, Carbon Comp. 330Ω, 1/4W, 5%	AB	CB3315	001090	4
R13, 14	Resistor, Carbon Comp. 820Ω, 1/4W, 5%	AB	CB8215	001097	2

PARTS LIST
DIGITAL OUTPUT BOARD
(OPTION P)

Reference	Description	Mfr.	Mfr. No.	EE No.	Qty.
	Digital Output PC Assembly	EE			
	Digital Output PC Board	EE	79-07141	047141	1
C1	Capacitor, Ceramic Disc .001 μF, 100 wvdc	SPR	TG-S10	000158	1
C2	Capacitor, Mylar .01 μF, 400 wvdc	AMPE	C280CF/P10K	000166	1
CR1,2	Diode, 1N3605	RAY	1N3605	000550	2
CR3,4	Diode, 3-1001	EE	3-1001	000570	2
J1	Connector, 50 pin	AML	57-40500	000443	1
Q1	Transistor, 2N3640	FAI	2N3640	001728	1
Q2,3	Transistor, 2N3646	FAI	2N3646	001731	2
R1	Resistor, Carbon Comp. 10k, 1/4W, 5%	AB	CB1035	001116	1
R2	Resistor, Carbon Comp. 3.9k, 1/4W, 5%	AB	CB3925	001108	1
R3,5,11,52, 53	Resistor, Carbon Comp. 1k, 1/4W, 5%	AB	CB1025	001098	4
R4	Resistor, Carbon Comp. 2.2k, 1/4W, 5%	AB	CB2225	001103	1
R6	Resistor, Carbon Comp. 220Ω, 1/4W, 5%	AB	CB2215	001086	1
R7	Resistor, Carbon Comp. 330Ω, 1/4W, 5%	AB	CB3315	001090	1
R8,9	Resistor, Carbon Comp. 100Ω, 1/4W, 5%	AB	CB1015	001081	2
R10,12,13,14, 15,	Resistor, Carbon Comp. 3.3k, 1/4W, 5%	AB	CB3325	001107	5
R20-51	Resistor, Carbon Comp. 22k, 1/4W, 5%	AB	CB2235	001120	32
U1	Micromodule, MC836P Hex Inverter	MOT	MC826P	003613	1
U2	Micromodule, MC840P Hex Inverter	MOT	MC840P	003616	1
U3	Micromodule, MC1812P Exclusive OR Gates	MOT	MC1812P		1

PARTS LIST
FRONT PANEL

Reference	Description	Mfr.	Mfr. No.	EE No.	Qty.
DS3	Lamp, Incandescent 28V	DIAL	507-3917-145-600	003089	1
J2, 3	Connector, BNC	AUTO	025-B3600-75	000400	2
R1, 3, 62, 64	Resistor, Carbon Comp. 62Ω, 1/4W, 5%	AB	CB6205	001078	4
R2, 63	Resistor, Carbon Comp. 240Ω, 1/4W, 5%	AB	CB2415	001087	2
R4, 65	Resistor, Carbon Comp. 51Ω, 1/4W, 5%	AB	CB5105	001076	2
R5, 66	Resistor, Carbon Comp. 470Ω, 1/4W, 5%	AB	CB4715	001092	2
R17, 44	Potentiometer, 1k	EE	003439	003439	2
S3, 4	Switch, Slide DP3T	CONW	G-128S	001555	2
S5, 6	Switch, Dlide DPDT	CONW	G-126	000553	2
S8/R106	Switch/Potentiometer SPST, 1MΩ	EE	SB3796A	001012	1
S10	Switch, Pushbutton	GRAY	30-1	001583	1
S201	Switch, Slide DPDT	CONW	G-126	001553	1
XDS3	Lamp, Holder	EE		045516	1
	Polaroid Lens	EE		047149	1
	MODE Switch Shaft	EE		046331	1
	Knob, Black, w/Pointer	EE		003082	1
	Knob, Black	EE		003083	3

PARTS LIST
REAR PANEL

Reference	Description	Mfr.	Mfr. No.	EE No.	Qty.
B201	Fan	PAM	8500	003068	1
F201	Fuse, 3AG 1A, FB	LTTL	312001	000592	1
FL201	Filter, Line	POTT	5004-6075	003333	1
J3, 4, 6	Connector, Subminiature RF	SEA	51-045-0000	000249	3
J5	Connector, BNC	AML	UG-1094	000383	1
R103	Resistor, Carbon Comp. 390Ω, 1/4W, 5%	AB	GB3915	001091	1
R104	Resistor, Carbon Comp. 1.2k, 1/4W, 5%	AB	CB1225	001099	1
S9	Switch, Slide DPDT	CONW	G-126	001553	1
S202	Switch, Slide DPDT	SWT	46256LF	001588	1
T201	Transformer	EE	B-50-06960	046960	1
XF201	Post, fuse	EE		000617	1
	Filter, Air	EE		045437	1
	Screen, Air Filter	EE		045439	1

PARTS LIST
HEATSINK ASSEMBLY

Reference	Description	Mfr.	Mfr. No.	EE No.	Qty.
	Heat Sink Assembly	EE	B-45-08419	048419	1
Q203, 206, 212	Transistor, MJE370	MOT	MJE370	003273	3
Q209, 210	Transistor, MJE520	MOT	MJE520	003274	2

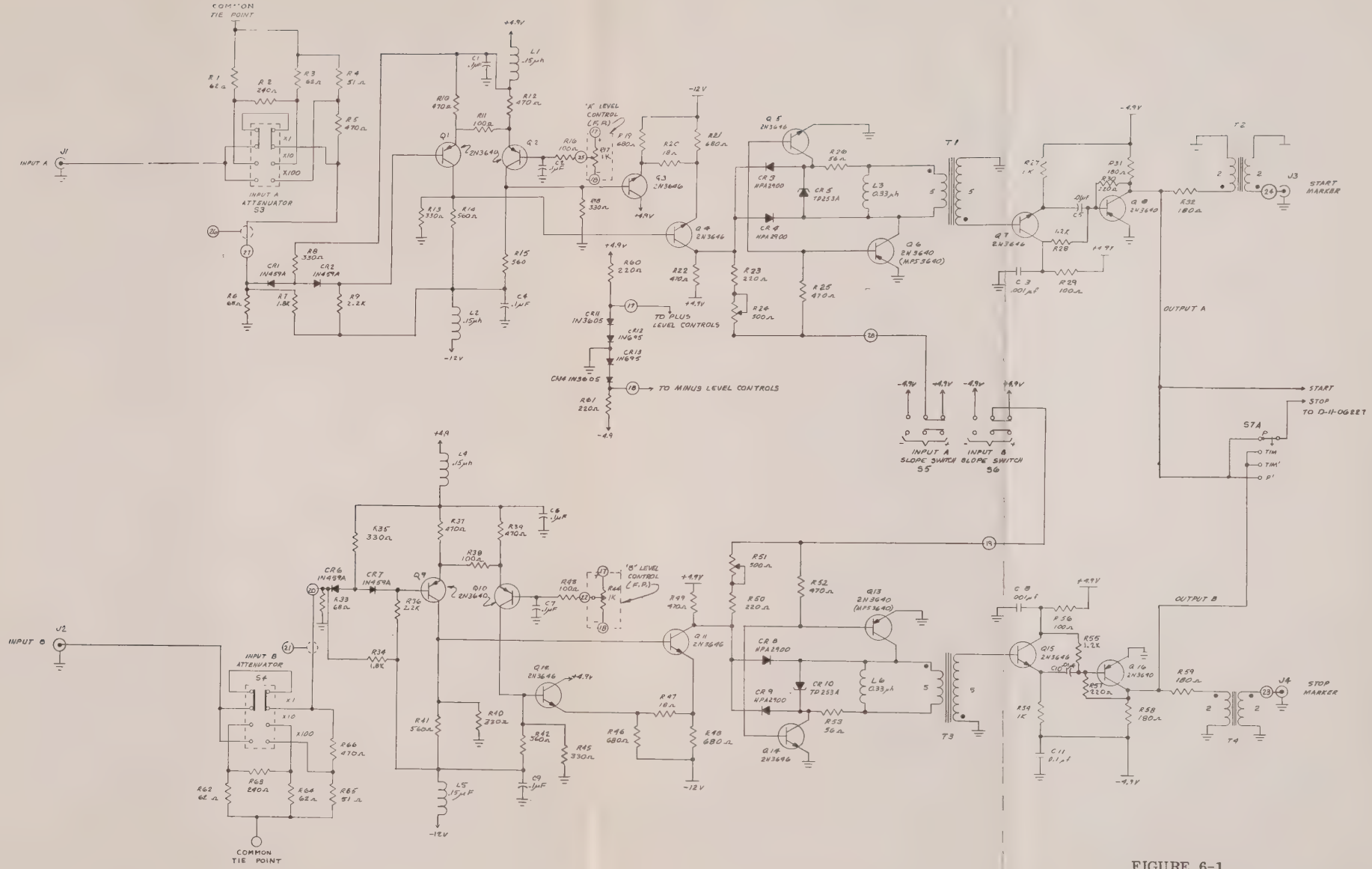


FIGURE 6-1
SCHEMATIC, INPUT CIRCUIT
(D-11-06226F)

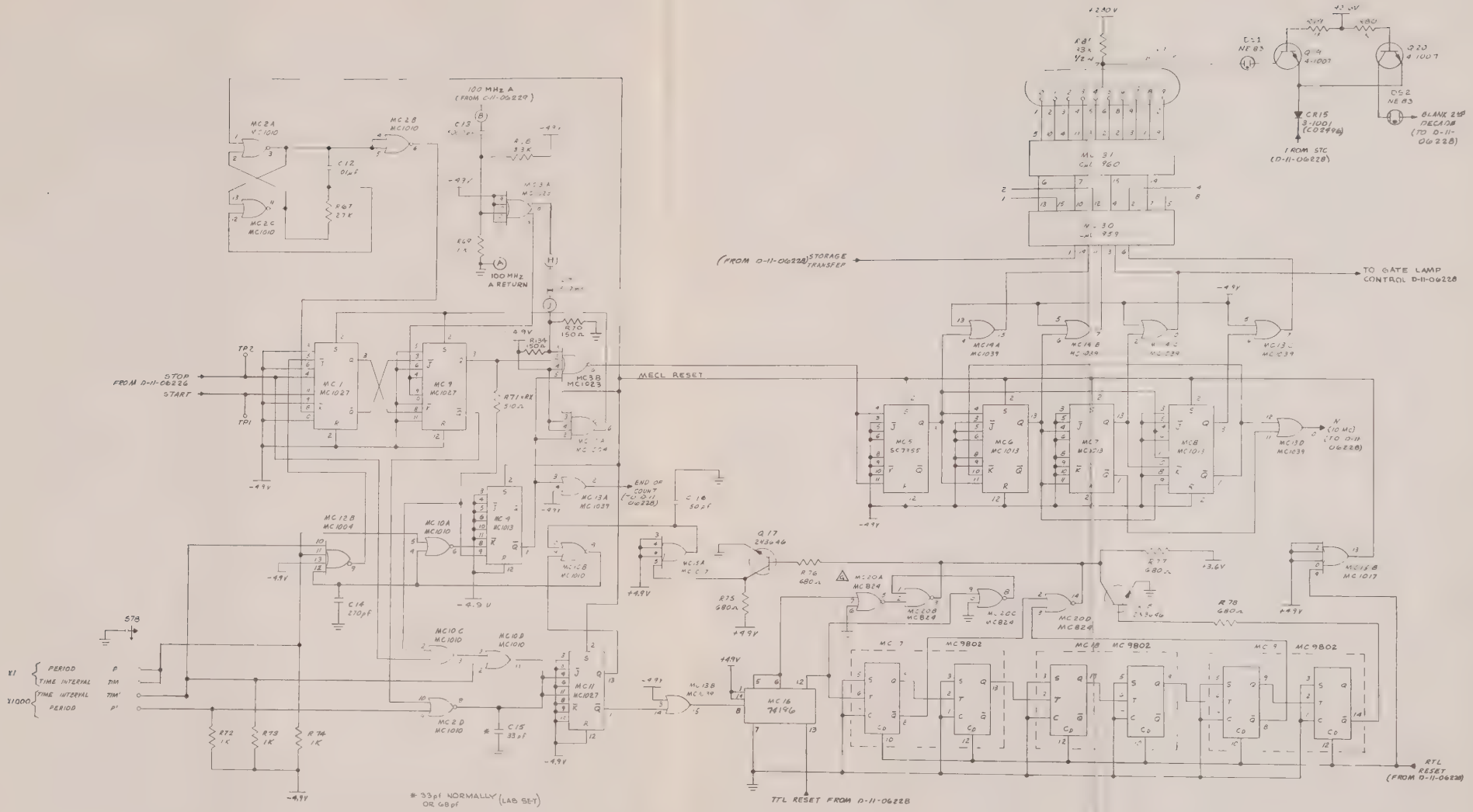


FIGURE 6-2
SCHEMATIC, STEERING LOGIC
(D-11-06227H)

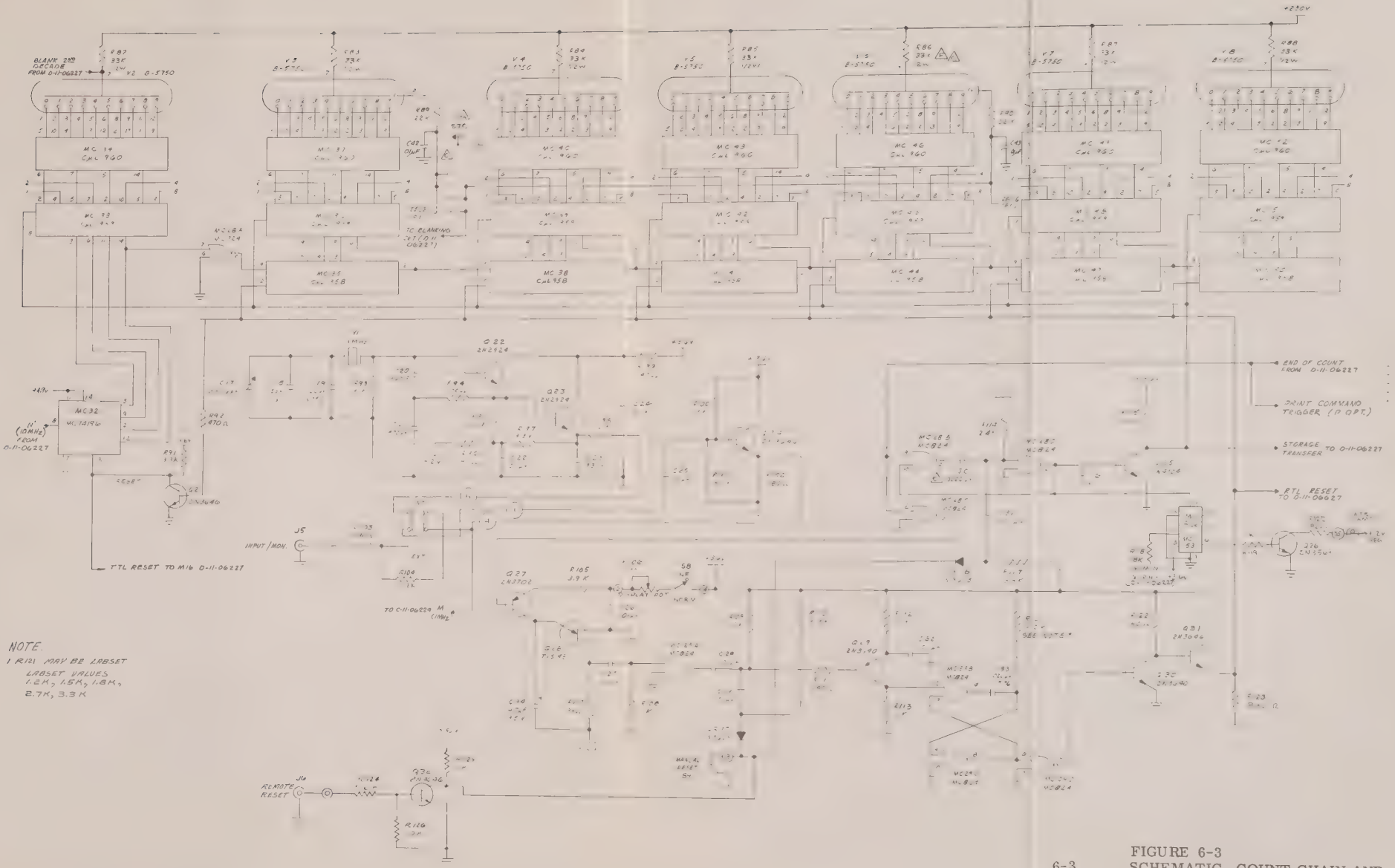


FIGURE 6-3
SCHEMATIC, COUNT CHAIN AND
RESET CIRCUITRY
(D-11-06628G)

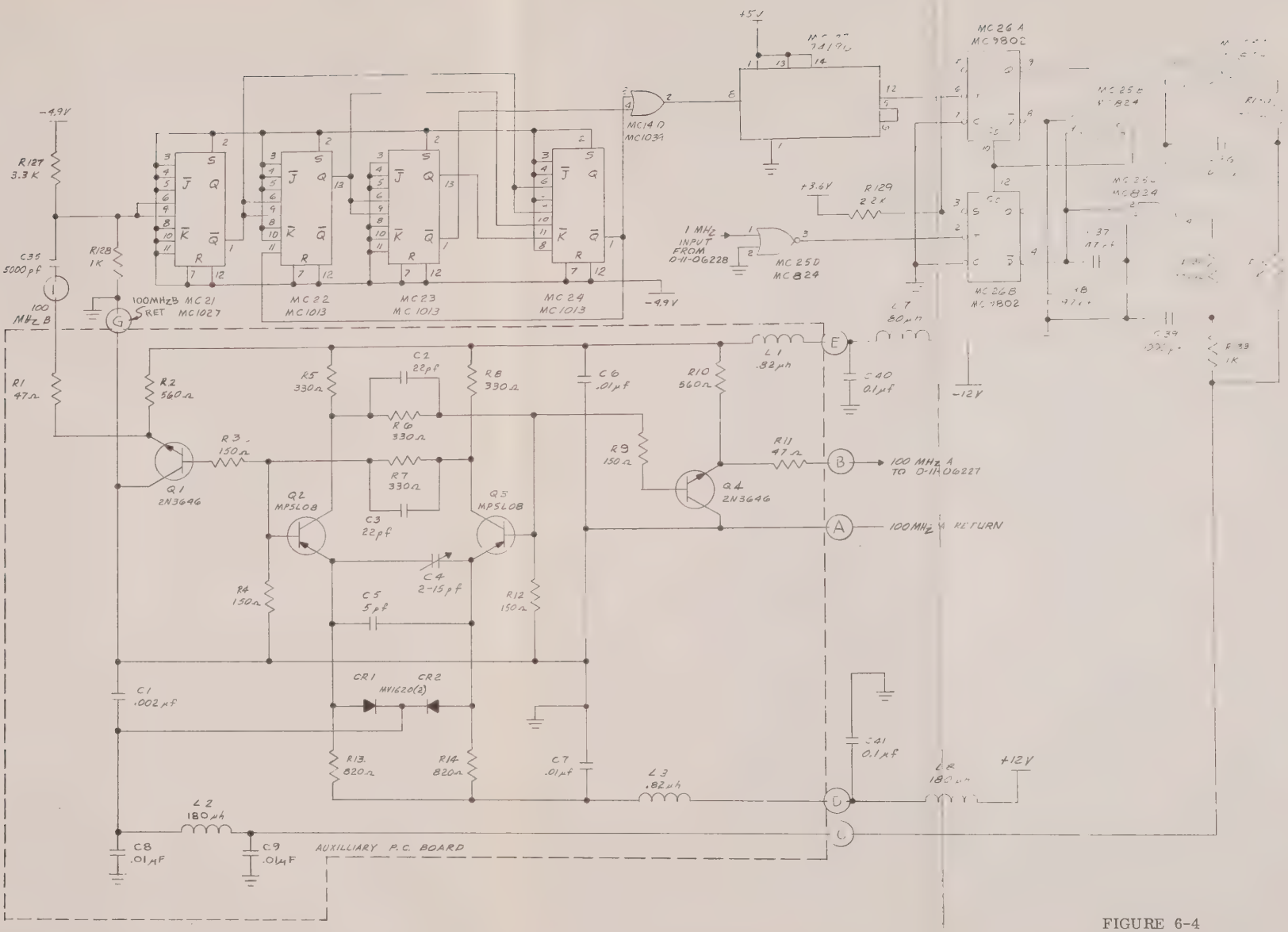


FIGURE 6-4
SCHEMATIC, 100 MHz VCO
(C-11-06229F)

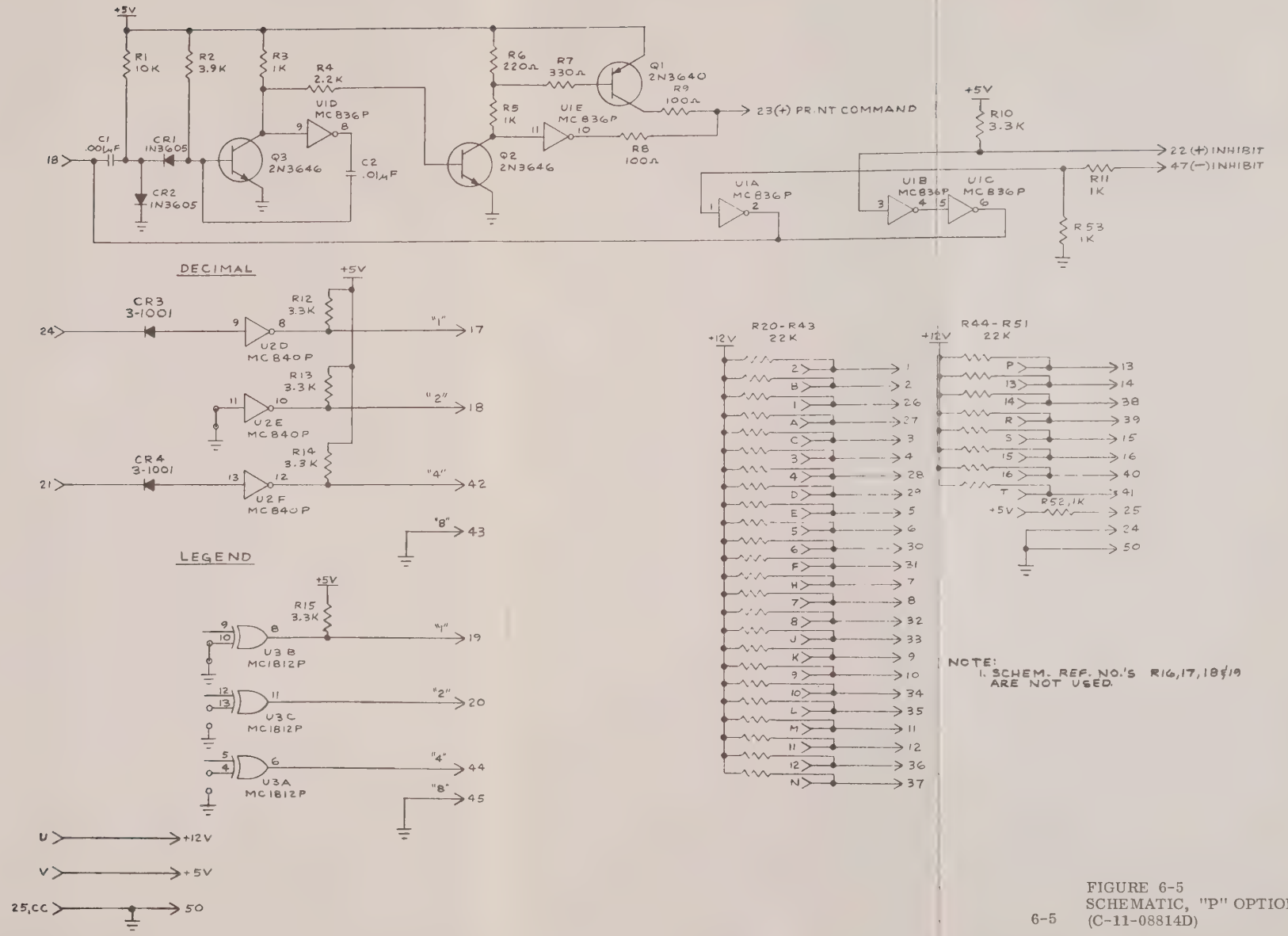


FIGURE 6-5
SCHEMATIC, "P" OPTION
(C-11-08814D)

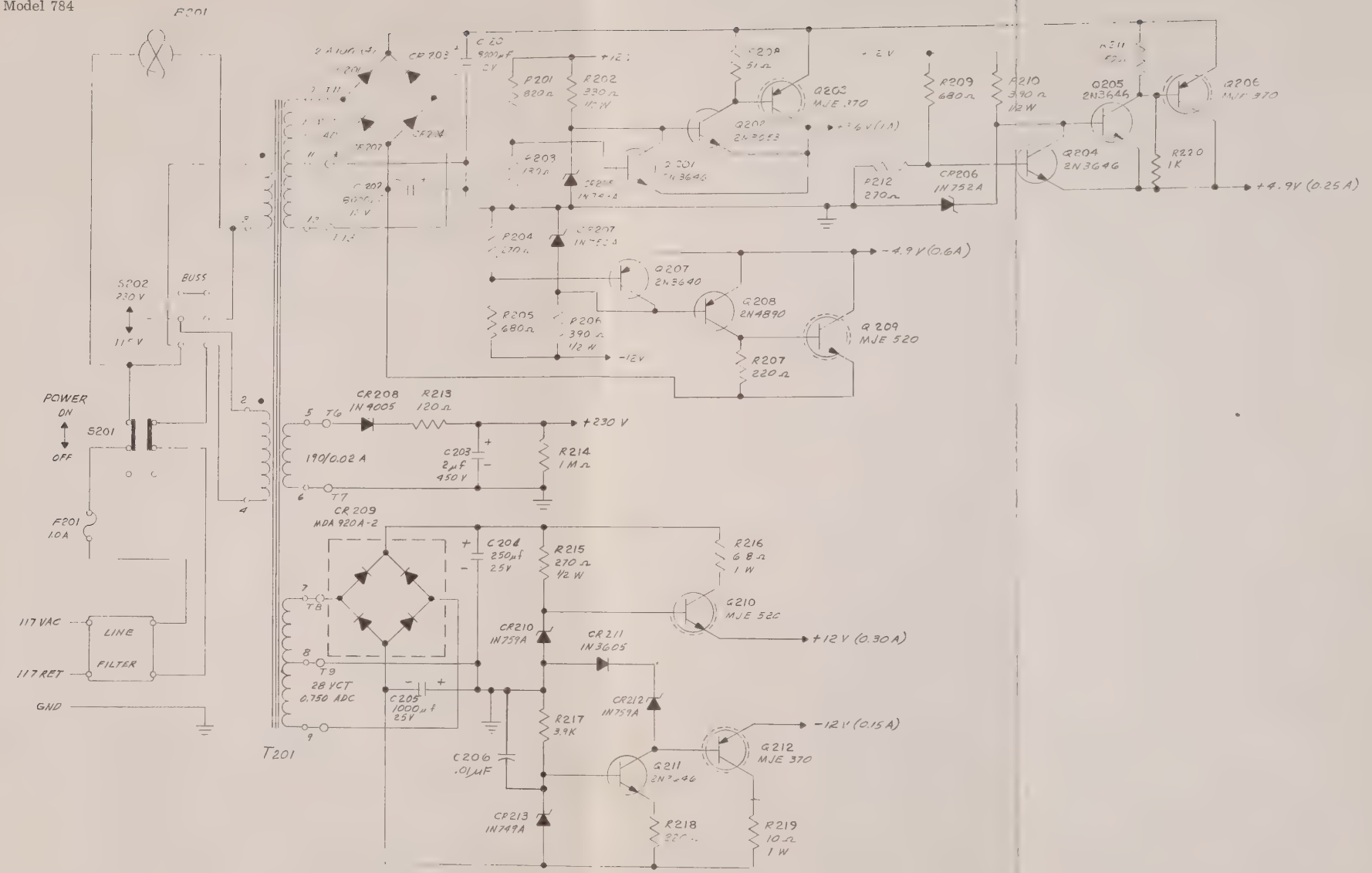


FIGURE 6-6
SCHEMATIC, POWER SUPPLY
(C-11-06226B)

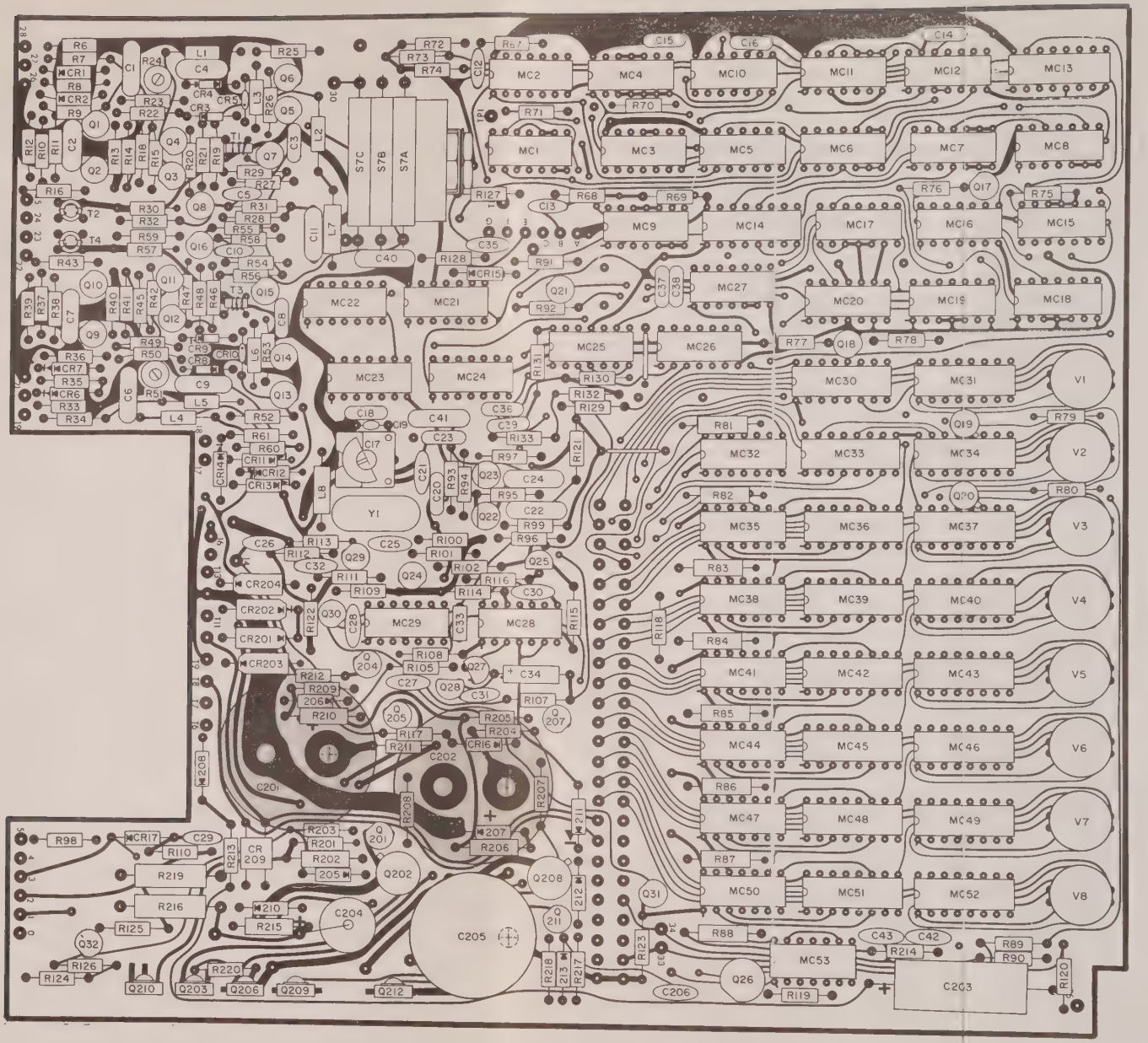


FIGURE 6-7
DISPLAY LOGIC P.C. BOARD
COMPONENT LOCATION DIAGRAM

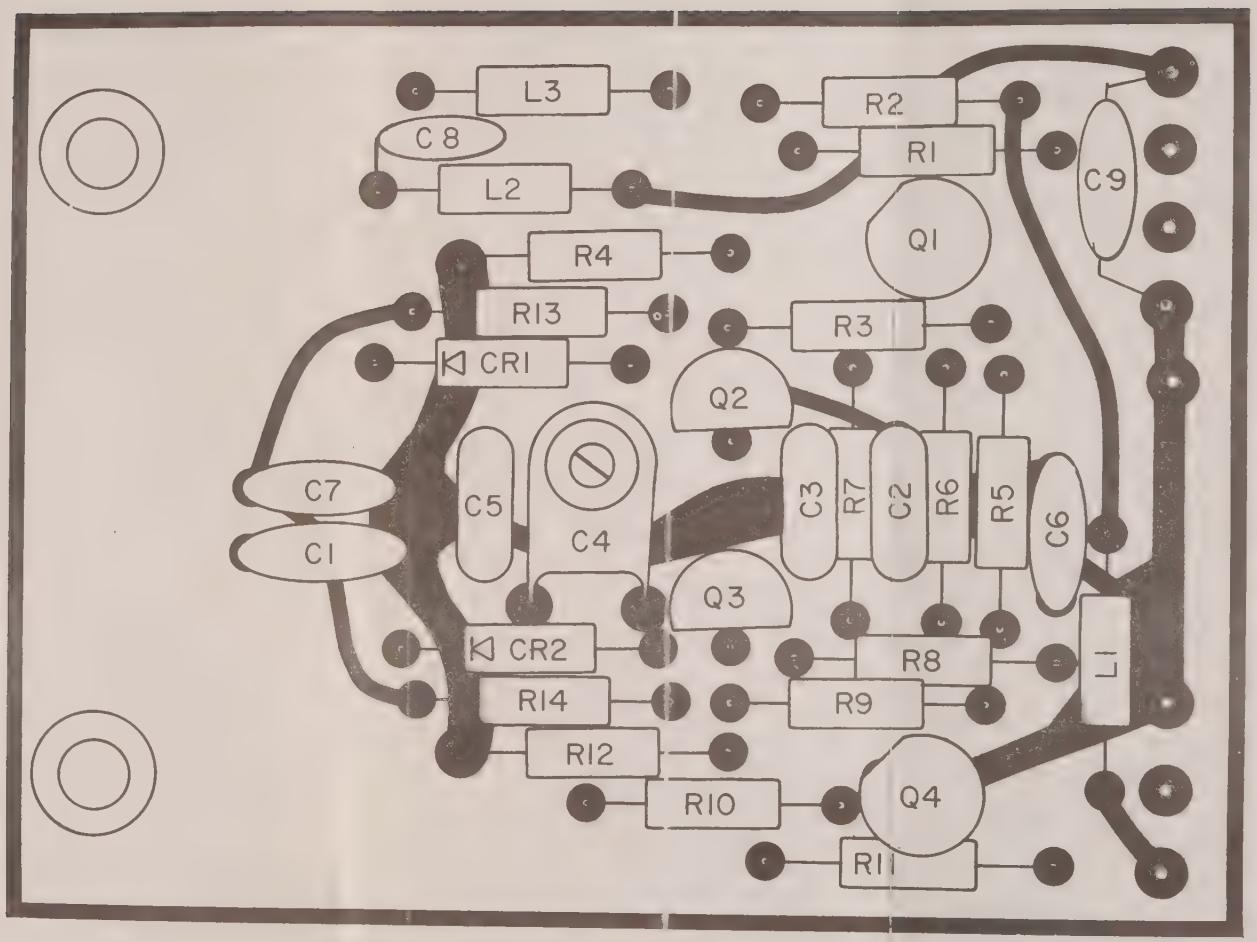


FIGURE 6-8
VCO P.C. BOARD
COMPONENT LOCATION DIAGRAM

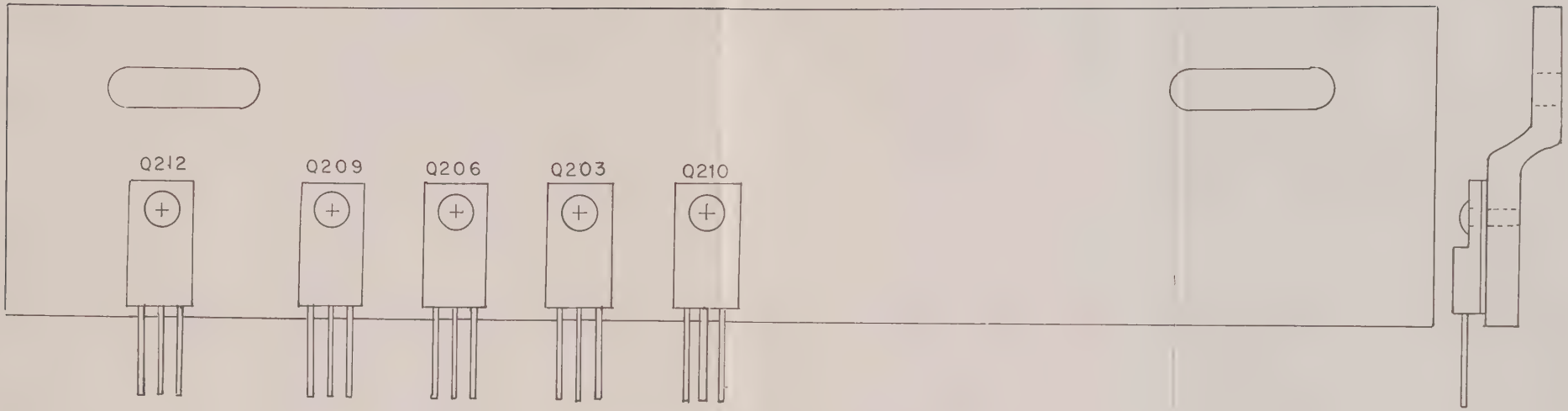
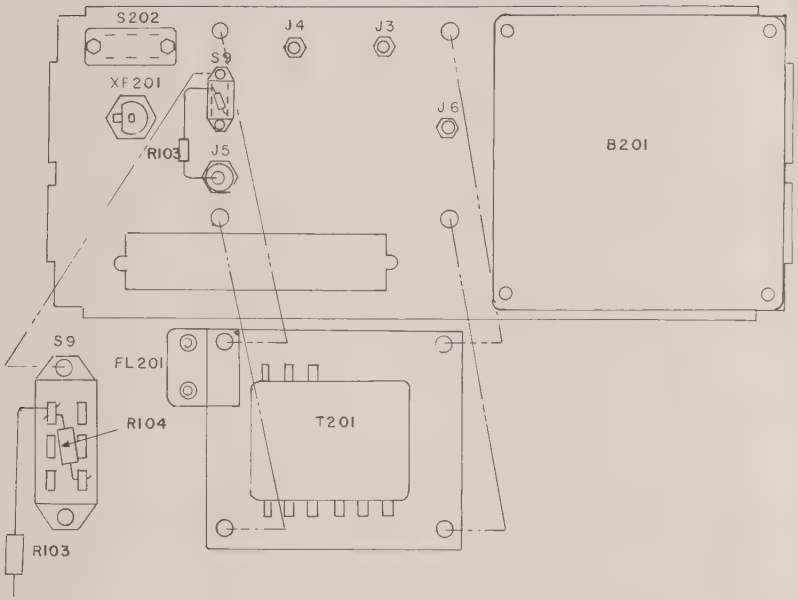


FIGURE 6-9
HEATSINK SUBASSEMBLY
COMPONENT LOCATION DIAGRAM



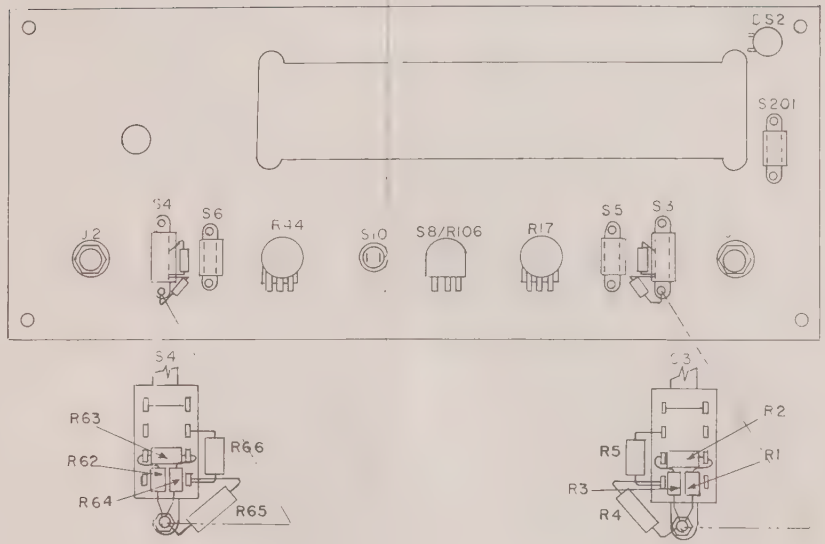


FIGURE 6-10
FRONT AND REAR PANEL
COMPONENT LOCATION DIAGRAM

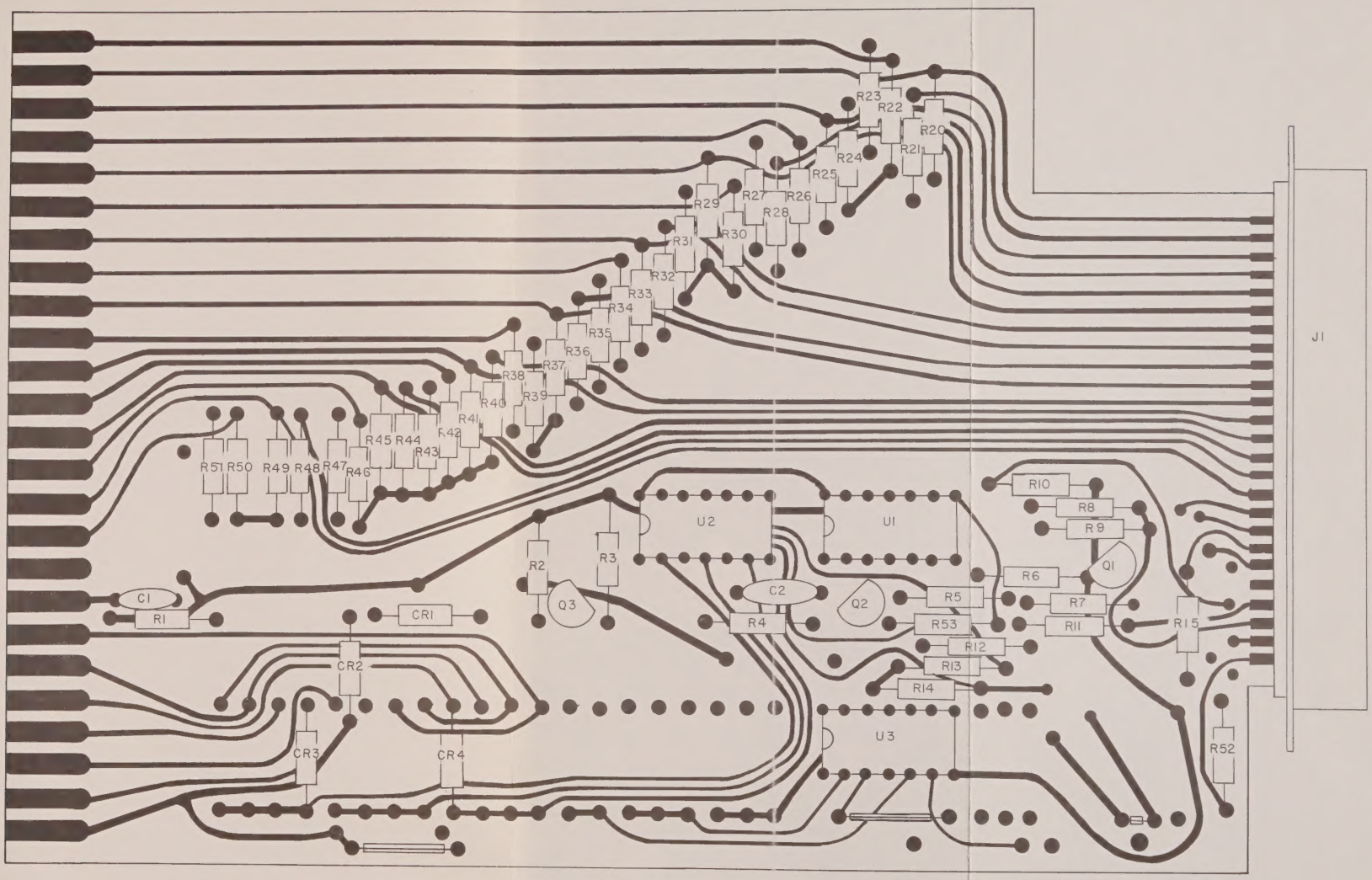


FIGURE 6-11
"P" OPTION P.C. BOARD
COMPONENT LOCATION DIAGRAM

MP MASTER
MA29723